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(74) Agent: EDWARDS, Gary, J.; Finnegan, Henderson,
Farabow, Garrett & Dunner LLP, 901 New York Avenue,
Washington, D.C., District of Columbia 20001-4413 (US).

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(71) Applicant (*for all designated States except US*): SYM-MORPHIX, INC. [US/US]; 1278 Reamwood Avenue, Sunnyvale, CA 94089-2233 (US).

(72) Inventors; and

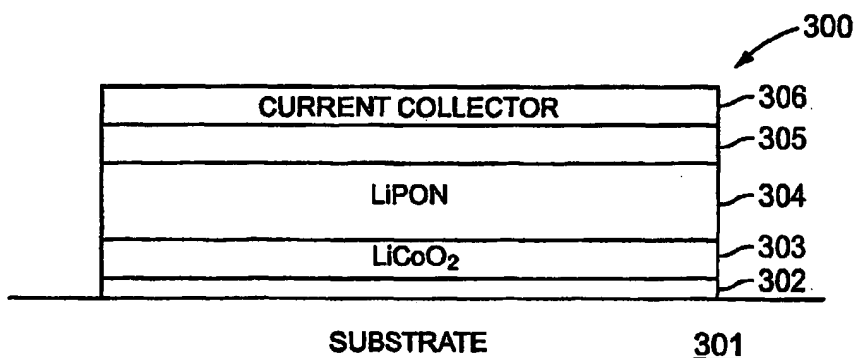
(75) Inventors/Applicants (*for US only*): ZHANG, Hongmei [US/US]; 1330 Rodney Drive, San Jose, CA 95118 (US). DEMARAY, Richard, E. [US/US]; 190 Fawn Lane, Portola Valley, CA 94028 (US). SHAO, May [US/US]; 5401 Nectar Circle, Elk Grove, CA 95757 (US).

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(54) Title: DEPOSITION OF LiCoO₂



(57) Abstract: In accordance with the present invention, deposition of LiCoO₂ layers in a pulsed-dc physical vapor deposition process is presented. Such a deposition can provide a low-temperature, high deposition rate deposition of a crystalline layer of LiCoO₂ with a desired <101> or <003> orientation. Some embodiments of the deposition addresses the need for high rate deposition of LiCoO₂ films, which can be utilized as the cathode layer in a solid state rechargeable Li battery. Embodiments of the process according to the present invention can eliminate the high temperature (>700°C) anneal step that is conventionally needed to crystallize the LiCoO₂ layer. Some embodiments of the process can improve a battery utilizing the LiCoO₂ layer by utilizing a rapid thermal anneal process with short ramp rates.

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DEPOSITION OF LiCoO_2

RELATED APPLICATION

[001] The present application claims priority to Provisional Application No. 60/651,363, filed on February 8, 2005, by Hongmei Zhang and Richard E. Demaray, and to Provisional Application No. 60/634,818, filed on December 8, 2004, by the same inventors, each of which are herein incorporated by reference in their entirety.

BACKGROUND

1. Field of the Invention

[002] The present invention is related to thin-film solid-state batteries and, in particular, the deposition of LiCoO_2 films and layers for battery manufacture.

2. Discussion of Related Art

[003] Solid-state thin-film batteries are typically formed by stacking thin films on a substrate in such a way that the films cooperate to generate a voltage. The thin films typically include current collectors, a cathode, an anode, and an electrolyte. The thin films can be deposited utilizing a number of deposition processes, including sputtering and electroplating. Substrates suitable for this application have conventionally been high temperature materials capable of withstanding at least one high temperature anneal process to at least 700 °C for up to about 2 hours in air so as to crystallize the LiCoO_2 film. Such a substrate can be any suitable material with appropriate structural and material properties, for example a semiconductor wafer, metallic sheet (e.g., titanium or zirconium), ceramic such as alumina, or other material capable of withstanding subsequent high temperature processing in

the presence of the LiCoO_2 , which can experience significant interfacial reactions with most materials utilized in a battery during these temperature cycles.

[004] Other lithium containing mixed metal oxides besides LiCoO_2 , including Ni, Nb, Mn, V, and sometimes also Co, but including other transition metal oxides, have been evaluated as crystalline energy storage cathode materials. Typically, the cathode material is deposited in amorphous form and then the material is heated in an anneal process to form the crystalline material. In LiCoO_2 , for example, an anneal at or above 700°C transforms the deposited amorphous film to a crystalline form. Such a high temperature anneal, however, severely limits the materials that can be utilized as the substrate, induces destructive reaction with the lithium containing cathode material and often requires the use of expensive noble metals such as gold. Such high thermal budget processes (i.e., high temperatures for extended periods of time) are incompatible with semiconductor or MEM device processing and limit the choice of substrate materials, increase the cost, and decrease the yield of such batteries. The inventors are unaware of a process disclosed in the art that allows production of cathodic lithium films for a battery structure where a post-deposition anneal process has a low enough thermal budget to allow production of functional structures on low temperature materials such as stainless steel, aluminum, or copper foil.

[005] It is known that crystallization of amorphous LiCoO_2 on precious metals can be achieved. An example of this crystallization is discussed in Kim et al., where a conventional furnace anneal at 700°C for 20 minutes of an amorphous layer of LiCoO_2 on a precious metal achieves crystallization of the LiCoO_2 material, as shown by x-ray diffraction data. Kim, Han-Ki and Yoon, Young Soo, "Characteristics of rapid-thermal-annealed LiCoO_2 cathode film for an all-solid-state thin film microbattery," J. Vac. Sci. Techn. A 22(4), Jul/Aug 2004. In Kim et al., the LiCoO_2 film was deposited on a platinum film that was deposited on a high-temperature MgO/Si substrate. In Kim et al, it was shown that such

a crystalline film is capable of constituting the Li⁺ ion containing cathode layer of a functional all solid-state Li⁺ ion battery. However, it is of continuing interest for the manufacture of solid state Li⁺ ion batteries to further reduce the thermal budget of the post deposition anneal, both in time and in temperature, so as to enable the manufacture of such batteries without the need for expensive precious metal nucleation, barrier layers, or expensive high-temperature substrates.

[006] There are many references that disclose an ion beam assisted process that can provide a LiCoO₂ film that demonstrates some observable crystalline composition by low angle x-ray diffraction (XRD). Some examples of these are found in U.S. Patent Applications 09/815,983 (Publication No. US 2002/001747), 09/815,621 (Publication No. US 2001/0032666), and 09/815,919 (Publication No. US 2002/0001746). These references disclose the use of a second front side ion beam or other ion source side-by-side with a deposition source so as to obtain a region of overlap of the flux of ions with the flux of LiCoO₂ vapor at the substrate surface. None of these references disclose film temperature data or other temperature data of the film during deposition to support an assertion of low temperature processing.

[007] It is very difficult to form a uniform deposition either by sputtering a material layer or by bombardment with an ion flux. Utilization of two uniform simultaneous distributions from two sources that do not occupy the same position and extent with respect to the substrate enormously increases the difficulties involved in achieving a uniform material deposition. These references do not disclose a uniform materials deposition, which is required for reliable production of thin-film batteries. A well understood specification for material uniformity for useful battery products is that a 5% one-sigma material uniformity is standard in thin film manufacturing. About 86% of the films with this uniformity will be found acceptable for battery production.

[008] It is even more difficult to scale a substrate to manufacturing scale, such as 200 mm or 300 mm. Indeed, in the references discussed above that utilize both a sputtering deposition and an ion beam deposition, only small area targets and small area substrates are disclosed. These references disclose a single feasibility result. No method for achieving a uniform distribution from two separate front side sources has been disclosed in these references.

[009] Further, conventional materials and production processes can limit the energy density capacity of the batteries produced, causing a need for more batteries occupying more volume. It is specifically desirable to produce batteries that have large amounts of stored energy per unit volume in order to provide batteries of low weight and low volume.

[010] Therefore, there is a need for a low temperature process for depositing crystalline material, for example LiCoO_2 material, onto a substrate.

SUMMARY

[011] In accordance with the present invention, deposition of LiCoO_2 layers in a pulsed-dc physical vapor deposition process is presented. Such a deposition can provide a low-temperature, high deposition rate deposition of a crystalline layer of LiCoO_2 with a desired $\langle 101 \rangle$ orientation. Some embodiments of the deposition address the need for high rate deposition of LiCoO_2 films, which can be utilized as the cathode layer in a solid state rechargeable Li battery. Embodiments of the process according to the present invention can eliminate the high temperature ($>700^\circ\text{C}$) anneal step that is conventionally needed to crystallize the LiCoO_2 layer.

[012] A method of depositing a LiCoO_2 layer according to some embodiments of the present invention includes placing a substrate in a reactor; flowing a gaseous mixture including argon and oxygen through the reactor; and applying pulsed-DC power to a target

formed of LiCoO_2 positioned opposite the substrate. In some embodiments, a LiCoO_2 layer is formed on the substrate. Further, in some embodiments the LiCoO_2 layer is a crystalline layer of orientation $\langle 101 \rangle$.

[013] In some embodiments, a stacked battery structure can be formed. The stacked battery structure includes one or more battery stacks deposited on a thin substrate, wherein each battery stack includes: a conducting layer, a crystalline LiCoO_2 layer deposited over the conducting layer, a LiPON layer deposited over the LiCoO_2 layer; and an anode deposited over the LiPON layer. A top conducting layer can be deposited over the one or more battery stacks.

[014] In some embodiments, a battery structure can be formed in a cluster tool. A method of producing a battery in a cluster tool includes loading a substrate into a cluster tool; depositing a conducting layer over the substrate in a first chamber of the cluster tool; depositing a crystalline LiCoO_2 layer over the conducting layer in a second chamber of the cluster tool; depositing a LiPON layer over the LiCoO_2 layer in a third chamber of the cluster tool; depositing an anode layer over the LiCoO_2 layer in a fourth chamber; and depositing a second conducting layer over the LiPON layer in a fifth chamber of the cluster tool.

[015] A fixture for holding a thin substrate can include a top portion and a bottom portion, wherein the thin substrate is held when the top portion is attached to the bottom portion.

[016] These and other embodiments of the invention are further discussed below with reference to the following figures. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed. Further, specific explanations or theories regarding the deposition or performance of certain layers during deposition processes or in the performance of devices incorporating those layers are presented for explanation only and

are not to be considered limiting with respect to the scope of the present disclosure or the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[017] Figures 1A and 1B illustrate a pulsed-DC biased reactive deposition apparatus that can be utilized in the methods of depositing according to the present invention.

[018] Figure 2 shows an example of a target that can be utilized in the reactor illustrated in Figures 1A and 1B.

[019] Figure 3 illustrates a thin-film battery design according to some embodiments of the present invention.

[020] Figures 4A and 4B show an x-ray diffraction analysis of and an SEM photograph of a LiCoO_2 film deposited according to embodiments of the present invention.

[021] Figures 5A through 5F show SEM photographs of LiCoO_2 films according to some embodiments of the present invention.

[022] Figure 5G shows x-ray diffraction data corresponding to the depositions shown in Figures 5B-5F.

[023] Figure 6A illustrates a layer of LiCoO_2 deposited according to some embodiments of the present invention on a thin substrate.

[024] Figure 6B illustrates a layer of LiCoO_2 deposited according to some embodiments of the present invention over a conducting layer on a thin substrate.

[025] Figures 7A, 7B, 7C, and 7D illustrate a thin substrate mount and mask arrangement that can be utilized in the deposition of LiCoO_2 layers deposited according to some embodiments of the present invention.

[026] Figure 8 illustrates a cluster tool that can be utilized to form batteries with LiCoO_2 layers deposited according to some embodiments of the present invention.

[027] Figures 9A and 9B illustrate examples of stacked battery structures with LiCoO_2 layers deposited according to some embodiments of the present invention.

[028] Figures 10A through 10D illustrate deposition and anneal steps for LiCoO_2 deposited over an iridium layer on a silicon wafer.

[029] Figures 11A through 11D illustrate a single layer battery formed over an iridium layer according to some embodiments of the present invention.

[030] Figures 12A through 12L illustrate deposition of a crystalline LiCoO_2 layer on a silicon or alumina substrate.

[031] Figures 13A through 13F illustrate rapid thermal anneal processes for LiCoO_2 layers deposited according to the present invention.

[032] Figures 14A through 14D illustrate several anneal processes utilized with a LiCoO_2 film deposited according to embodiments of the present invention.

[033] Figures 15A and 15B illustrate the effects of ramp-time in a rapid thermal anneal of LiCoO_2 films deposited according to the present invention.

[034] Figure 16 illustrates thickness uniformity of a LiCoO_2 film deposited according to some embodiments of the present invention.

[035] Figure 17 illustrates battery charge and discharge profiles of a battery formed utilizing a LiCoO_2 film according to some embodiments of the present invention.

[036] In the figures, elements having the same designation have the same or similar functions.

DETAILED DESCRIPTION

[037] In accordance with embodiments of the present invention, LiCoO_2 films are deposited on a substrate by a pulsed-dc physical vapor deposition (PVD) process. In contrast to, for example, Kim et al., LiCoO_2 films according to some embodiments of the present

invention provide a crystalline LiCoO_2 film as deposited on a substrate at a substrate temperature as low as about 220°C during deposition, without the use of a metallic nucleation or barrier underlying film. The as-deposited crystalline LiCoO_2 films can be easily ripened to very high crystalline condition by anneal at about 700°C for as little as 5 minutes without the use of an underlying precious metal film. In addition, the as deposited crystalline films, when positioned on a noble metal film can be annealed at much further reduced temperatures, for example as low as 400 to 500°C , providing for deposition, annealing, and production of solid state batteries on lower temperature substrates.

[038] In the present application, a single, extended source is described which has been scaled to $400\text{mm} \times 500\text{mm}$ for production achieving a LiCoO_2 uniformity of 3% one-sigma measured at 25 points at a deposition rate of 1.2 microns thickness an hour over an area of 2000 cm^2 , without the need for secondary front side ion source or ion assistance.

[039] In one example process, a LiCoO_2 film was deposited utilizing a conductive ceramic LiCoO_2 target as described herein, with pulsed-dc power of 4 kW, no bias, with 60 sccm Ar and 20 sccm O_2 gas flows. A 3000 Angstrom layer of crystalline LiCoO_2 was deposited on a substrate area of $400 \times 500\text{ mm}$. As demonstrated in Figure 16, film thickness uniformity was located at about 25 locations spaced uniformly across the substrate using a felt marker pen to lift off a portion of the film in each location. High precision white-light interferometry was utilized to measure the film thickness in each location by measuring the step height from the substrate to film surface. All 25 thickness measurements demonstrated a 3% one-sigma uniformity in the film thickness over $400 \times 500\text{ mm}$ substrate area. As shown in Figure 16, a film was deposited with average thickness of about $2.96\text{ }\mu\text{m}$ with a maximum of $3.09\text{ }\mu\text{m}$ and a minimum of $2.70\text{ }\mu\text{m}$ and standard deviation of 0.093. Thickness data was taken at points spaced 0.65 mm apart on the surface of the film. The film thickness therefore showed 3% one-sigma uniformity over the shown surface area.

[040] On other depositions utilizing this process, a temperature measurement of the substrate during deposition showed that the substrate remained at less than 224 °C.

Temperature measurements were performed utilizing a temperature sticker purchased from Omega Engineering, Stamford, Ct (Model no. TL-F-390, active from 199-224 °C).

[041] Moreover, in some embodiments, films deposited according to the present invention can have a deposition rate of from about 10 to about 30 times higher than processes in conventional films. Deposition thicknesses and times of deposition for films deposited according to the present invention are illustrated in Table I. Furthermore, films according to the present invention can be deposited on wide area substrates having a surface area from 10 to 50 times the surface area of prior sputtering processes, resulting in much higher productivity and much lower cost of manufacture, thereby providing high-volume, low-cost batteries.

[042] Further, conventional deposition processes without ion sources are capable of depositing amorphous LiCoO_2 layers, but do not deposit crystalline LiCoO_2 layers. Surprisingly, depositions according to some embodiment of the present invention, deposit a LiCoO_2 layer with substantial crystallinity readily measured by x-ray diffraction techniques. In some embodiments, the crystallinity of the as-deposited LiCoO_2 layers is sufficient to be utilized in a battery structure with no further thermal processing. In some embodiments, crystallinity of the as-deposited LiCoO_2 layers are improved by thermal processes with low thermal budgets, which can be compatible with films deposited on low-temperature substrates.

[043] Further, as-deposited the stoichiometry of some LiCoO_2 layers deposited according to some embodiments of the present invention shows that this layer is sufficient for utilization in a battery. With the demonstrated ability to deposit a LiCoO_2 film with crystallinity and with sufficient stoichiometry, a battery utilizing as-deposited LiCoO_2 films

can be produced. Heat treating the LiCoO_2 layers may improve the crystallinity and lower the impedance.

[044] In some embodiments, a crystalline layer of LiCoO_2 with a $\langle 101 \rangle$ or a $\langle 003 \rangle$ crystalline orientation is deposited directly on the substrate. Deposition of crystalline material can eliminate or lessen the need of a subsequent high temperature anneal or precious-metal layers to crystallize and orient the film. Removing the high temperature anneal allows for formation of battery structures on light-weight and low temperature substrates such as stainless steel foil, copper foil, aluminum foil, and plastic sheet, reducing both the weight and the cost of batteries while retaining the energy density storage capabilities of Li-based batteries. In some embodiments, a crystalline LiCoO_2 layer can be deposited on a precious metal layer, such as platinum or iridium, resulting in a further significant lowering of the ripening thermal budget required to improve crystallinity.

[045] Deposition of materials by pulsed-DC biased reactive ion deposition is described in U.S. Patent Application Serial No. 10/101863, entitled "Biased Pulse DC Reactive Sputtering of Oxide Films," to Hongmei Zhang, et al., filed on March 16, 2002. Preparation of targets is described in U.S. Patent Application Serial No. 10/101,341, entitled "Rare-Earth Pre-Alloyed PVD Targets for Dielectric Planar Applications," to Vassiliki Milonopoulou, et al., filed on March 16, 2002. U.S. Patent Application Serial No. 10/101863 and U.S. Patent Application Serial No. 10/101,341 are each assigned to the same assignee as is the present disclosure and each is incorporated herein in their entirety. Deposition of oxide materials has also been described in U.S. Patent No. 6,506,289, which is also herein incorporated by reference in its entirety. Transparent oxide films can be deposited utilizing processes similar to those specifically described in U.S. Patent No. 6,506,289 and U.S. Application Serial No. 10/101863.

[046] Figure 1A shows a schematic of a reactor apparatus 10 for sputtering material from a target 12 according to the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three deposition chambers connected by a vacuum transport chamber. These AKT reactors can be modified such that pulsed DC power is supplied to the target and RF power is supplied to the substrate during deposition of a material film. Apparatus 10 can also be a Phoenix Gen III PVD cluster tool made by Symmorphix, which is specifically designed for pulsed-dc processes such as is described herein.

[047] Apparatus 10 includes target 12 which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on a substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it from the pulsed DC power supply 14 and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18. A magnet 20 is scanned across the top of target 12.

[048] For pulsed reactive dc magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the positive period, the insulating layer on the surface of target 12 is discharged and arcing is prevented. To obtain arc free deposition, the pulsing frequency exceeds a critical frequency that can depend on target material, cathode current and reverse time. High quality oxide films can be made using reactive pulse DC magnetron sputtering as shown in apparatus 10.

[049] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this DC power supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 kHz. The reverse voltage can be 10% of the negative target voltage. Utilization of other power supplies can lead to different power characteristics, frequency characteristics, and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted between 0 and 5 μ s.

[050] Filter 15 prevents the bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 can be a 2 MHz RF power supply, for example a Nova-25 power supply made by ENI, Colorado Springs, Co.

[051] In some embodiments, filter 15 can be a 2 MHz sinusoidal band rejection filter. In some embodiments, the band width of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 14 and allow passage of the pulsed-dc power and frequency.

[052] Pulsed DC deposited films are not fully dense and may have columnar structures. Columnar structures can be detrimental to thin film applications such as barrier films and dielectric films, where high density is important, due to the boundaries between the columns. The columns act to lower the dielectric strength of the material, but may provide diffusion paths for transport or diffusion of electrical current, ionic current, gas, or other chemical agents such as water. In the case of a solid state battery, a columnar structure containing crystallinity as derived from processes according to the present invention is beneficial for battery performance because it allows better Li transport through the boundaries of the material.

[053] In the Phoenix system, for example, target 12 can have an active size of about 800.00 X 920.00 mm by 4 to 8 mm in order to deposit films on substrate 16 that have

dimension about 600 X 720 mm. The temperature of substrate 16 can be adjusted to between -50 °C and 500 °C. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm (in some embodiments, between 4.8 and 6 cm are used). Process gas can be inserted into the chamber of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about .7 and 6 milli Torr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the Phoenix reactor, magnet 20 can be a race-track shaped magnet with dimensions about 150 mm by 800 mm.

[054] Figure 2 illustrates an example of target 12. A film deposited on a substrate positioned on carrier sheet 17 directly opposed to region 52 of target 12 has good thickness uniformity. Region 52 is the region shown in Figure 1B that is exposed to a uniform plasma condition. In some implementations, carrier 17 can be coextensive with region 52. Region 24 shown in Figure 2 indicates the area below which both physically and chemically uniform deposition can be achieved, for example where physical and chemical uniformity provide refractive index uniformity, oxide film uniformity, or metallic film uniformity. Figure 2 indicates region 52 of target 12 that provides thickness uniformity, which is, in general, larger than region 24 of target 12 providing thickness and chemical uniformity to the deposited film. In optimized processes, however, regions 52 and 24 may be coextensive.

[055] In some embodiments, magnet 20 extends beyond area 52 in one direction, for example the Y direction in Figure 2, so that scanning is necessary in only one direction, for example the X direction, to provide a time averaged uniform magnetic field. As shown in Figures 1A and 1B, magnet 20 can be scanned over the entire extent of target 12, which is larger than region 52 of uniform sputter erosion. Magnet 20 is moved in a plane parallel to the plane of target 12.

[056] The combination of a uniform target 12 with a target area 52 larger than the area of substrate 16 can provide films of highly uniform thickness. Further, the material properties of the film deposited can be highly uniform. The conditions of sputtering at the target surface, such as the uniformity of erosion, the average temperature of the plasma at the target surface, and the equilibration of the target surface with the gas phase ambient of the process are uniform over a region which is greater than or equal to the region to be coated with a uniform film thickness. In addition, the region of uniform film thickness is greater than or equal to the region of the film which is to have highly uniform electrical, mechanical, or optical properties such as index of refraction, stoichiometry, density, transmission, or absorptivity.

[057] Target 12 can be formed of any materials that provide the correct stoichiometry for LiCoO_2 deposition. Typical ceramic target materials include oxides of Li and Co as well as metallic Li and Co additions and dopants such as Ni, Si, Nb, or other suitable metal oxide additions. In the present disclosure, target 12 can be formed from LiCoO_2 for deposition of LiCoO_2 film.

[058] In some embodiments of the invention, material tiles are formed. These tiles can be mounted on a backing plate to form a target for apparatus 10. A wide area sputter cathode target can be formed from a close packed array of smaller tiles. Target 12, therefore, may include any number of tiles, for example between 2 and 60 individual tiles. Tiles can be finished to a size so as to provide a margin of edge-wise non-contact, tile to tile, less than about 0.010" to about 0.020" or less than half a millimeter so as to eliminate plasma processes that may occur between adjacent ones of tiles 30. The distance between tiles of target 12 and the dark space anode or ground shield 19 in Figure 1B can be somewhat larger so as to provide non contact assembly or to provide for thermal expansion tolerance during process chamber conditioning or operation.

[059] As shown in Figure 1B, a uniform plasma condition can be created in the region between target 12 and substrate 16 in a region overlying substrate 16. A plasma 53 can be created in region 51, which extends under the entire target 12. A central region 52 of target 12 can experience a condition of uniform sputter erosion. As discussed further herein, a layer deposited on a substrate placed anywhere below central region 52 can then be uniform in thickness and other properties (i.e., dielectric, optical index, or material concentrations). In some embodiments, target 12 is substantially planar in order to provide uniformity in the film deposited on substrate 16. In practice, planarity of target 12 can mean that all portions of the target surface in region 52 are within a few millimeters of a planar surface, and can be typically within 0.5 mm of a planar surface.

[060] Figure 3 shows a battery structure with a LiCoO_2 layer deposited according to some embodiments of the present invention. As shown in Figure 3, a metallic current collection layer 302 is deposited on a substrate 301. In some embodiments, current collection layer 302 can be patterned in various ways before deposition of a LiCoO_2 layer 303. Also according to some embodiments, LiCoO_2 layer 303 can be a deposited crystalline layer. In some embodiments of the invention, layer 303 is crystalline without the necessity of a crystallizing heat treatment. Therefore, substrate 301 can be a silicon wafer, titanium metal, alumina, or other conventional high temperature substrate, but may also be a low temperature material such as plastic, glass, or other material which could be susceptible to damage from the high temperature crystallizing heat treatment. This feature can have the great advantage of decreasing the expense and weight of battery structures formed by the present invention. The low temperature deposition of the LiCoO_2 allows for successive depositions of battery layers, one upon another. Such a process would have the advantage that successive layers of battery structure would be obtained in a stacked condition without the inclusion of a substrate

layer. The stacked layered battery would provide higher specific energy density as well as low impedance operation for charging and discharging.

[061] In some embodiments, an oxide layer can be deposited on substrate 301. For example, a silicon oxide layer can be deposited on a silicon wafer. Other layers can be formed between conducting layer 302 and substrate 301.

[062] As further shown in Figure 3, a LiPON layer 304 ($\text{Li}_x\text{PO}_y\text{N}_z$) is deposited over LiCoO_2 layer 303. LiPON layer 304 is the electrolyte for battery 300 while LiCoO_2 layer 303 acts as the cathode. A metallic conducting layer 305 can be deposited over the LiPON layer 304 in order to complete the battery. Metallic conducting layer 305 can include lithium adjacent to LiPON layer 304.

[063] An anode 305 is deposited over LiPON layer 304. Anode 305 can be, for example an evaporated lithium metal. Other materials such as, for example, nickel can also be utilized. A current collector 306, which is a conducting material, is then deposited over at least a portion of anode 305.

[064] A Li based thin film battery operates by transport of Li ions in the direction from current collector 306 to current collector 302 in order to hold the voltage between current collector 306 and current collector 302 at a constant voltage. The ability for battery structure 300 to supply steady current, then, depends on the ability of Li ions to diffuse through LiPON layer 304 and LiCoO_2 layer 303. Li transport through bulk cathode LiCoO_2 layer 303 in a thin film battery occurs by the way of grains or grain boundaries. Without being restricted in this disclosure to any particular theory of transport, it is believed that the grains with their planes parallel to substrate 302 will block the flow of Li ions while grains oriented with planes perpendicular to substrate 301 (i.e., oriented parallel to the direction of Li ion flow) facilitate the Li diffusion. Therefore, in order to provide a high-current battery

structure, LiCoO_2 layer 303 should include crystals oriented in the $\langle 101 \rangle$ direction or $\langle 003 \rangle$ direction.

[065] In accordance with the present invention, LiCoO_2 films can be deposited on substrate 302 with a pulsed-DC biased PVD system as was described above. In addition, an AKT 1600 PVD system can be modified to provide an RF bias, which is available in the Phoenix system, and an Advanced Energy Pinnacle plus 10K pulsed DC power supply can be utilized to provide power to a target. The pulsing frequency of the power supply can vary from about 0 to about 350 KHz. The power output of the power supply is between 0 and about 10 kW. A target of densified LiCoO_2 tiles having a resistivity in the range of about 3 to about $10 \text{ k}\Omega$ can be utilized with dc-sputtering.

[066] In some embodiments, LiCoO_2 films are deposited on Si wafers. Gas flows containing Oxygen and Argon can be utilized. In some embodiments, the Oxygen to Argon ratio ranges from 0 to about 50% with a total gas flow of about 80 sccm. The pulsing frequency ranges from about 200 kHz to about 300 kHz during deposition. RF bias can also be applied to the substrate. In many trials, the deposition rates vary from about 2 Angstrom/(kW sec) to about 1 Angstrom/(kW sec) depending on the O_2/Ar ratio as well as substrate bias.

[067] Table I illustrates some example depositions of LiCoO_2 according to the present invention. XRD (x-Ray Diffraction) results taken on the resulting thin films illustrate that films deposited according to the present invention are crystalline films, often with highly textured grain sizes as large as about 150 nm. The dominant crystal orientation appears to be sensitive to the O_2/Ar ratio. For certain O_2/Ar ratios ($\sim 10\%$), as-deposited films exhibit a preferred orientation in the $\langle 101 \rangle$ direction or the $\langle 003 \rangle$ direction with poorly developed $\langle 003 \rangle$ planes.

[068] Figures 4A and 4B illustrate an XRD Analysis and SEM cross section, respectively, of the LiCoO_2 film deposited as Example 15 in Table I. Such a LiCoO_2 film was deposited on Si wafer with 2kW of target power, a frequency of 300 kHz, with 60 sccm Ar and 20 sccm of O_2 for a substrate with an initial temperature of about 30°C. As shown in the XRD analysis of Figure 4A, a strong $\langle 101 \rangle$ peak is indicated showing a strong orientation of LiCoO_2 crystals in the desired $\langle 101 \rangle$ crystallographic direction. The SEM cross section shown in Figure 4B further shows the columnar structure of the film having the $\langle 101 \rangle$ direction and the grain boundaries of the resulting LiCoO_2 crystals.

[069] Figures 5A through 5F show SEM cross sections of further example depositions of LiCoO_2 crystals according to the present invention. In each of the examples, deposition of the LiCoO_2 film was performed on a Si wafer with target power of about 2 kW and frequency of about 250 kHz. The LiCoO_2 film shown in Figure 5A corresponds to the example deposition Example 1 in Table I. In the deposition of the LiCoO_2 film shown in Figure 5A, no bias power was utilized with an argon flow rate of about 80 sccm and an oxygen flow rate of about 0 sccm. A deposition rate of about 1.45 $\mu\text{m/hr}$ was achieved over the full substrate area of 400 X 500 mm. Further, as is indicated in the cross section shown in Figure 5A, a $\langle 101 \rangle$ orientation of the LiCoO_2 was achieved.

[070] The rate of deposition of the LiCoO_2 layer shown in Figure 5A is very high, likely due to the relatively high conductivity or low resistivity of the ceramic LiCoO_2 oxide sputter target. A target resistance of 10 kOhms was measured by means of an Ohm meter over a distance of about 4 cm on the surface of target 12. This high rate allows the manufacture of the 3 micron or thicker LiCoO_2 layer required for the battery at high rate over a wide area in short times, resulting in very high productivity and very low cost. Target resistance on the order of about 500 k Ω over the same distance by the same measurement technique or higher would not allow for such a high sputter efficiency or high rate of

deposition at such a low target power. The resistance of conventional target materials can be unmeasurably high. A resistance of 100 k Ω over about 4 cm of surface will result in high sputter efficiency and high rate of deposition. Further, because deposition rates typically scale nearly linearly with target power, a deposition at 6 kW will yield a deposition rate of approximately 3 $\mu\text{m/hr}$, which is a very desirable rate of deposition for manufacturability of Li-based thin-film solid-state batteries on a surface area of 400 X 500 mm².

[071] The LiCoO₂ layer shown in Figure 5B is deposited under the conditions listed as Example 7 in Table I. Again, no bias was utilized in the deposition. An argon flow rate of about 72 sccm and an oxygen flow rate of about 8 sccm was utilized. The deposition rate was significantly reduced to about 0.85 $\mu\text{m/hr}$. Further, although a <101> crystallinity can be discerned, that <101> crystallinity is not as pronounced as that exhibited in the deposition of the film shown in Figure 5A.

[072] The LiCoO₂ film shown in Figure 5C was deposited according to Example 3 in Table I. In this deposition, 100 W of bias power is applied to the substrate. Further, an argon flow rate of 72 sccm, and an oxygen flow rate of 8 sccm was utilized. The deposition rate was about 0.67 $\mu\text{m/hr}$. Therefore, the application of bias in comparison with the LiCoO₂ film shown in Figure 5B further reduced the deposition rate (from 0.85 $\mu\text{m/hr}$ of the example shown in Figure 5B to 0.67 $\mu\text{m/hr}$ of the example shown in Figure 5C). Further, the desired <101> directionality of formed crystals appears to be further degraded.

[073] The LiCoO₂ film shown in Figure 5D corresponds to Example 4 in Table I. In this deposition, the Ar/O₂ ratio was increased. As is shown in Figure 5D, increasing the Ar/O₂ ratio improves crystallinity. With respect to the example illustrated in Figure 5C, the deposition illustrated in Figure 5D was performed with an argon flow of about 76 sccm and an oxygen flow of about 4 sccm as well as retaining the 100 W bias to the substrate. The

LiCoO₂ deposition rate was improved to 0.79 $\mu\text{m/hr}$ from a rate of 0.67 $\mu\text{m/hr}$ illustrated in Figure 5C.

[074] In the example deposition illustrated in Figure 5E corresponding to Example 5 in Table I. The substrate temperature was set at about 200°C while the bias power remained at about 100 W. The argon flow rate was set at about 76 sccm and the oxygen flow rate was set at about 4 sccm. The resulting deposition rate for the LiCoO₂ layer was about 0.74 $\mu\text{m/hr}$.

[075] In the example deposition illustrated in Figure 5F, which corresponds with Example 6 of Table I, the argon flow rate was set at about 74 sccm and the oxygen flow rate was set at about 6 sccm, resulting in a LiCoO₂ deposition rate of about 0.67 $\mu\text{m/hr}$. Therefore, increasing both argon and oxygen flow rate over the deposition illustrated in Figure 5E resulted in a lower deposition rate.

[076] Figure 5G illustrates XRD data corresponding to Figures 5F, 5D, 5C, 5E, and 5B, respectively. As illustrated in Figure 5G, as-deposited crystalline LiCoO₂ is deposited in these processes.

[077] The data show clearly that an as-deposited crystalline film of LiCoO₂ can be obtained under several of the process conditions, as shown in Table II. In particular, very high rates of deposition with low power are obtained along with the oriented crystalline structure for the process conditions according to embodiments of the present invention.

[078] Figure 6A illustrates a layer of LiCoO₂ 602 deposited on a thin substrate 601 according to some embodiments of the present invention. Higher lithium-ion mobilities can be achieved utilizing crystalline LiCoO₂ cathode films 602 deposited on a thin substrate 601 that has thickness comparable to that of the battery stack itself, rather than a thickness many or tens of times that of the battery stack. Such a film can lead to faster charging and discharging rates. Substrate 601 can be formed of a thin metallic sheet (e.g., aluminum,

titanium, stainless steel, or other suitable thin metallic sheet), can be formed of a polymer or plastic material, or may be formed of a ceramic or glass material. As shown in Figure 6B, if substrate 601 is an insulating material, a conducting layer 603 can be deposited between substrate 601 and LiCoO_2 layer 602.

[079] Depositing materials on a thin substrate involves holding and positioning the substrate during deposition. Figures 7A, 7B, 7C, and 7D illustrate a reusable fixture 700 for holding a thin film substrate. As shown in Figure 7A, reusable fixture 700 includes a top portion 701 and a bottom portion 702 that snap together. Thin substrate 601 is positioned between top portion 701 and bottom portion 702. As shown in Figure 7B, top portion 701 and bottom portion 702 are such that substrate 601 is brought into tension and subsequently clamped as top portion 701 is closed into bottom portion 702. Substrate 601 can be easily held by fixture 700 so that substrate 601 can be handled and positioned. In some embodiments, the corners of substrate 601, areas 703, are removed so that substrate 601 is more easily stretched by avoiding "wrap-around" corner clamping effects when top portion 701 is closed into bottom portion 702.

[080] As shown in Figure 7C, a mask 712 can be attached to fixture 700. In some embodiments, fixture 700 includes guides in order to align fixture 700 with respect to mask 712. In some embodiments, mask 712 may be attached to fixture 700 and travel with fixture 700. Mask 712 can be positioned at any desired height above substrate 601 in fixture 700. Therefore, mask 712 can function as either a contact or proximity mask. In some embodiments, mask 712 is formed of another thin substrate mounted in a fixture similar to fixture 700.

[081] As shown in Figure 7C and 7D, fixture 700 and mask 712 can be positioned relative to mount 710. Mount 710, for example, can be a susceptor, mount, or an electrostatic chuck of a processing chamber such as that shown in Figures 1A and 1B. Fixture 700 and

mask 712 can have features that allow for ready alignment with respect to each other and with respect to mount 710. In some embodiments, mask 712 is resident in the processing chamber and aligned with fixture 700 during positioning of fixture 700 on mount 710, as shown in Figure 7D.

[082] Utilizing fixture 700 as shown in Figures 7A, 7B, 7C, and 7D allows processing of a thin film substrate in a processing chamber. In some embodiments, thin film substrates can be about 10 μm or more. Further, thin film substrate 601, once mounted within fixture 700, can be handled and moved from process chamber to process chamber. Therefore, a multiprocessor chamber system can be utilized to form stacks of layers, including one or more layers of LiCoO_2 deposited according to embodiments of the present invention.

[083] Figure 8 illustrates a cluster tool 800 for processing thin film substrates. Cluster tool 800 can, for example, include load lock 802 and load lock 803, through which mounted thin film substrate 601 is loaded and a resultant device is removed from cluster tool 800. Chambers 804, 805, 806, 807, and 808 are processing chambers for depositions of materials, heat treatments, etching, or other processes. One or more of chambers 804, 805, 806, 807, and 808 can be a pulsed-DC PVD chamber such as that discussed above with respect to Figures 1A and 1B and within which a LiCoO_2 film deposited according to embodiments of the present invention may be deposited.

[084] Processing chambers 804, 805, 806, 807, and 808 as well as load locks 802 and 803 are coupled by transfer chamber 801. Transfer chamber 801 includes substrate transfer robotics to shuttle individual wafers between processing chambers 804, 805, 806, 807, and 808 and load locks 802 and 803.

[085] In production of a conventional thin-film battery, ceramic substrates are loaded into load lock 803. A thin metallic layer can be deposited in chamber 804, followed

by a LiCoO_2 deposition performed in chamber 805. The substrate is then removed through load lock 803 for an in-air heat treatment external to cluster tool 800. The treated wafer is then reloaded into cluster tool 800 through load lock 802. A LiPON layer can be deposited in chamber 806. The wafer is then again removed from cluster tool 800 for deposition of the lithium anode layer, or sometimes chamber 807 can be adapted to deposition of the lithium anode layer. A second metallic layer is deposited in chamber 808 to form a charge collector and anode collector. The finished battery structure is then off-loaded from cluster tool 800 in load lock 802. Wafers are shuttled from chamber to chamber by robotics in transfer chamber 801.

[086] A battery structure produced according to the present invention could utilize thin film substrates loaded in a fixture such as fixture 700. Fixture 700 is then loaded into load lock 803. Chamber 804 may still include deposition of a conducting layer. Chamber 805 then includes deposition of a LiCoO_2 layer according to embodiments of the present invention. A LiPON layer can then be deposited in chamber 806. Chamber 807 may still be adapted to deposition of a lithium rich material such as lithium metal and chamber 808 can be utilized for deposition of the conducting layer of the current collector. In this process, no heat treatment is utilized to crystallize the LiCoO_2 layer.

[087] Another advantage of a thin film battery process is the ability to stack battery structures. In other words, substrates loaded into cluster tool 800 may traverse process chambers 804, 805, 806, 807, and 808 multiple times in order to produce multiply stacked battery structures. Figures 9A and 9B illustrate such battery structures.

[088] Figure 9A illustrates a parallel coupled stacking. As shown in Figure 9A, a substrate 601, which for example can be a plastic substrate, is loaded into load lock 803. A conducting layer 603, for example about $2\ \mu\text{m}$ of aluminum, copper, iridium or other material, acts as a bottom current collector. Conducting layer 603, for example, can be

deposited in chamber 804. A LiCoO_2 layer 602 is then deposited on conducting layer 603. LiCoO_2 layer 602 can be about 3-10 μm and can be deposited in chamber 805 according to embodiments of the present invention. The wafer can then be moved to chamber 806 where a LiPON layer 901 of thickness of about .5 to about 2 μm can be deposited. In chamber 807, an anode layer 902, for example a lithium metal layer of up to about 10 μm , can then be deposited in chamber 807. A second conducting layer 903 can then be deposited over anode layer 902. A second battery stack can then be deposited over the first battery stack formed by metal layer 603, LiCoO_2 layer 602, LiPON layer 901, lithium layer 902, and current collection conduction layer 903. Over current collection conducting layer 903, another lithium layer 902 is formed. Another LiPON layer 901 is formed over lithium layer 902. Another LiCoO_2 layer 602 is formed over LiPON layer 901 and finally another metal layer 603 is formed over LiCoO_2 layer 602. In some embodiments, further stackings can be formed. In some embodiments, metal layers 603 and 903 differ in the mask utilized in deposition so that tabs are formed for electrical coupling of layers.

[089] As discussed above, any number of individual battery stacks can be formed such that parallel battery formations are formed. Such a parallel arrangement of battery stacking structure can be indicated as Current collector/ LiCoO_2 /LiPON/Anode/current collector/Anode/LiPON/ LiCoO_2 /current collector/ LiCoO_2 . . . /current collector. Figure 9B illustrates an alternative stacking corresponding to the battery structure current collector/ LiCoO_2 /LiPON/anode/current collector/ LiCoO_2 /LiPON/anode/current collector . . . /current collector. In this case, a series arrangement battery stacking structure is formed because the individual battery stacks share anodes.

[090] To form the structures shown in Figures 9A and 9B, substrates are rotated again through the chambers of cluster tool 800 in order to deposit the multiple sets of batteries. In general, a stack of any number of batteries can be deposited in this fashion.

[091] In some embodiments, stoichiometric LiCoO_2 can be deposited on iridium. Figures 10A through 10D illustrate an anneal procedure for Li-Co deposition over an iridium layer that has been deposited on a Si wafer. The LiCoO_2 deposition was accomplished as discussed above with a target power of 2 kW, no bias power, reverse time of 1.6 μs , a pulsing frequency of 300 kHz, with 60 sccm Ar flow and 20 sccm of O_2 flow, with no pre-heat for 7200 sec. As a result, a layer of LiCoO_2 of about 1.51 μm was deposited.

[092] Figures 10A through 10D show XRD analysis of both as-deposited and annealed layers of LiCoO_2 deposited as discussed above. The XRD analysis of the as-deposited layer demonstrates a shallow peak at $2\theta = 18.85^\circ$ denoting a $\langle 003 \rangle$ orientation of crystalline LiCoO_2 , a sharper peak at about $2\theta = 38.07^\circ$ corresponding with the desired $\langle 101 \rangle$ crystallographic direction, and a peak at $2\theta = 40.57^\circ$ corresponding to the $\langle 111 \rangle$ direction of iridium. However, the position of the $\langle 101 \rangle$ LiCoO_2 peak indicates that the $\langle 101 \rangle$ LiCoO_2 peak is nonstoichiometric LiCoO_2 . In order to be useful as a battery layer, stoichiometric LiCoO_2 provides for the best Li transport. One of ordinary skill in the art will notice that careful adjustment of deposition parameters can provide stoichiometric LiCoO_2 of desired orientation.

[093] Figure 10B shows an XRD analysis of the sample shown in figure 10A after a 300°C anneal in air for 2 hours. As shown in Figure 10B, the XRD peak corresponding to $\langle 003 \rangle$ LiCoO_2 grows, indicating crystallization of LiCoO_2 into the $\langle 003 \rangle$ direction. Further, the $\langle 101 \rangle$ peak of LiCoO_2 shifts slightly to $2\theta = 38.53^\circ$, indicating a more stoichiometric crystallization of the $\langle 101 \rangle$ LiCoO_2 . However, the crystalline LiCoO_2 is still not stoichiometric after this anneal. One of ordinary skill in the art will notice that longer anneals and/or further adjustment of the deposited stoichiometry may result in usefully oriented stoichiometric LiCoO_2 layers with anneal temperatures at 300°C or less. Consequently, low temperature materials such as polymers, glass, or metal may be utilized as the substrate.

[094] Figure 10C illustrates an XRD analysis from the sample after a subsequent 500°C anneal in air for 2 hours. As shown in Figure 10C, more of the LiCoO_2 crystallizes into the $\langle 003 \rangle$ layer. Further, the $\langle 101 \rangle$ LiCoO_2 peak shifts again to $2\theta = 39.08^\circ$, indicating crystallization of a $\langle 012 \rangle$ layer of LiCoO_2 . In this case, the $\langle 012 \rangle$ LiCoO_2 crystal is stoichiometric and therefore allows for efficient Li transport. One of ordinary skill in the art will notice that longer anneals and/or further adjustment of the deposited stoichiometry may result in usefully oriented stoichiometric LiCoO_2 layers with anneal temperatures at 500°C or less. Consequently, low temperature materials such as polymers, glass, or metal may be utilized as the substrate.

[095] Figure 10D illustrates an XRD analysis of the sample after a subsequent anneal of 700°C in air for 2 hours. As shown in Figure 10D, the $\langle 003 \rangle$ LiCoO_2 peak disappears, but the $\langle 012 \rangle$ LiCoO_2 peak remains relatively the same as that shown in the 500°C anneal illustrated in Figure 10C.

[096] Figures 10A through 10D demonstrate deposition of $\langle 101 \rangle$ LiCoO_2 at low temperature over an iridium layer. Subsequent anneals to 500°C may be desired to change the stoichiometry of the $\langle 101 \rangle$ LiCoO_2 layer, but anneals to 700 °C do not appear to be necessary. With anneal temperatures less than 500°C, depositions of a LiCoO_2 layer over a conducting iridium layer can be accomplished on glass, aluminum foil, plastic, or other low temperature substrate material. Anneal temperatures of less than 500°C but greater than 300°C or lengthening the time of lower temperature anneals may also result in desired orientations of stoichiometric crystalline LiCoO_2 .

[097] Figures 11A through 11D illustrate formation of a single-layer battery according to some embodiments of the present invention. As shown in Figure 11A, a lift-off layer 1102 can be deposited on a substrate 1101. Further, an iridium layer 1103 can be

deposited over lift-off layer 1102. In some embodiments, substrate 1101 can be plastic, glass, Al foil, Si wafer, or any other material. Lift-off layer 1102 can be any lift off layer and can be a polymer layer such as polyimide, an inorganic layer such as CaF_2 or carbon, or an adhesive layer that loses its adhesion as a result of, for example, oxidation, heat, or light. Lift-off layers are well known. Iridium layer 1103 can be from about 500 Å or more.

[0098] As shown in Figure 11B, a LiCoO_2 layer is deposited over iridium layer 1103 as was discussed above. In some embodiments, an anneal can be performed at this step. In some embodiments, further layers of the battery may be deposited before an anneal step is performed. In some embodiments, a stoichiometric LiCoO_2 layer of a useful crystalline orientation may result in the as-deposited LiCoO_2 with no further anneals necessary.

[0099] Figure 11C illustrates deposition of a LiPON layer 1105 over the LiCoO_2 layer, deposition of a Li layer 1106 over LiPON layer 1105, and deposition of an electrode layer 1107 over Li layer 1106. In some embodiments, an anneal step of up to 500°C as discussed above may be performed here.

[0100] As shown in Figure 11D, the resulting single-layer battery formed from iridium layer 1103, LiCoO_2 layer 1104, LiPON layer 1105, Li layer 1106, and electrode layer 1107 can be "lifted off" from substrate 1101. Such a single-layer battery can be a free-standing battery of thickness about 5 μm or greater. Such a battery, without the requirement of a substrate 1101, is well known to have the potential of energy storage of greater than about 1 kW-hr/liter.

[0101] As an alternative to a lift-off process as described in Figures 11A through 11D, a substrate may be removed during anneal leaving a single-layer battery. Further, in some embodiments, substrate 1101 can be removed by a solvent, etching, or a photo process. Further, single-layer batteries may be combined or stacked in any fashion to provide a device of greater energy storage at a particular voltage.

[0102] Figures 12A through 12L illustrate the crystallinity of as-grown and post anneal LiCoO_2 layers according to samples 31 and 32 illustrated in Table I. Samples 31 and 32 were formed in the same deposition, utilizing a silicon substrate and an alumina substrate, respectively.

[0103] Figure 12A illustrates an XRD analysis of the as-deposited LiCoO_2 film on Al_2O_3 substrate (Example 32 in Table I). A broad $\langle 003 \rangle$ crystalline LiCoO_2 peak is observed. The remaining peaks in the analysis, which are not labeled in Figure 12A, result from the Al_2O_3 substrate. The $\langle 003 \rangle$ peak is characteristic of the layered structure in the as-deposited crystalline LiCoO_2 film according to embodiments of the present invention.

[0104] Figure 12B illustrates the crystallinity of the LiCoO_2 film shown in Figure 12A after a 2 hr 700 °C anneal. As shown in Figure 12B, the $\langle 003 \rangle$ peak becomes sharper and higher, indicating better crystallinity. As shown in Figures 12G through 12J, in comparison with figures 12C through 12F, the columnar structure ripens with the anneal and the grain size becomes larger with anneal. Figure 12B also shows $\langle 012 \rangle$ and $\langle 006 \rangle$ crystallinity peaks.

[0105] Figure 12C through 12F show SEM photos of the granularity of the as-deposited film corresponding to Example 32 in Figure I. Figures 12G through 12J show SEM photos of the granularity of the annealed film, as illustrated in Figure 12B. A comparison of Figures 12C through 12F with 12G through 12J illustrate the increased granularity resulting from the anneal process.

[0106] Figure 12K illustrates a fracture cross-section SEM that illustrates the morphology of the as-deposited crystalline film corresponding to Example 31 in Table I. Figure 12L illustrate a similar cross-section SEM corresponding to the film grown according to Example 32 in Table I.

[0107] Figures 13A through 13J illustrate rapid thermal anneal processes applied to a LiCoO_2 layer as in Example 49 of Table I. In that example, LiCoO_2 is deposited on alumina with a 2 kW pulsed DC power with no bias. Argon flow as set to 60 sccm and oxygen flow was set to 20 sccm. The deposition parameters are nearly identical with those of Example 32 in Table I, therefore XRD data for the as-deposited films are shown in Figure 12A. Figure 13A shows XRD data after a 15 minute 700 °C anneal in an argon atmosphere. Ramp-up time (room temperature to 700 °C) is 45 sec and ramp-down time (700 °C to about 300 °C) occurred over 10 min. At 300 °C, the sample is removed from the rapid-thermal-anneal (RTA) oven and cooled in air to room temperature. As shown in Figure 13A, substantial crystallinity is obtained. Figure 13B shows XRD data after a RTA as described with Figure 13A in an argon/oxygen atmosphere. The argon/oxygen ratio was 3:1.

[0108] As shown in a comparison of Figures 13A and 13B, more crystallinity is observed in an argon only RTA than with a RTA performed in the presence of oxygen. This is further illustrated in a comparison of Figures 13C and 13D with Figures 13E and 13F. Figures 13C and 13D show the granularity of the LiCoO_2 film after the RTA illustrated in Figure 13A. Figures 13E and 13F show the granularity of the LiCoO_2 film after the RTA illustrated in Figure 13B. As is observed, the granularity shown in Figures 13C and 13D (which differ in magnification) is better than that shown in Figures 13E and 13F (which also differ in magnification).

[0109] Figures 14A through 14D illustrate several anneal processes with the Example 37 of Table I. In that example, LiCoO_2 was deposited on alumina utilizing a pulsed-dc process with 2kW of power and 100 W of bias with an argon flow of 60 sccm and an oxygen flow of 20 sccm.

[0110] Figure 14A shows an SEM photo of an as-deposited LiCoO_2 film according to the process illustrated in Example 37 of Table I. Figure 14B shows an SEM photo of

LiCoO₂ film according to the process illustrated in Example 37 of Table I, annealed conventionally with a two-hour 700 °C anneal. Figures 14C and 14D show SEM photos of a LiCoO₂ film according to the process illustrated in Example 37 of Table I, annealed in an RTA process at 700 °C. The ramp-up and ramp-down times in the RTA process is illustrated above. Figure 14C shows an SEM photo of a LiCoO₂ film after an RTA process at 700 °C for five minutes whereas Figure 14D shows an SEM photo of a LiCoO₂ film after an RTA process at 700 °C for fifteen minutes. It is clear from a comparison of Figures 14C and 14D with Figure 14B, that much better granularity is achieved with the low thermal-budget RTA process rather than the conventional furnace anneal. A low thermal-budget RTA process allows for deposition of such films on low temperature substrates.

[0111] Figures 15A and 15B show SEM photos of a LiCoO₂ film that was annealed in an RTA process utilizing two different ramp-up times, illustrating the effects of the ramp time in the RTA process. A LiCoO₂ film was deposited on an alumina substrate according to the process described as Example 51 in Table I. The film shown in Figure 15A was annealed with a 45 sec ramp-up time (i.e., room temperature to 700 °C in 45 sec). The film shown in Figure 15B was annealed with a 240 sec ramp-up time. Both films were held at 700 °C for five minutes. As shown in a comparison between Figures 15A and 15B, it is clear that a short anneal ramp-up times yield better granularity than longer ramp-up times.

[0112] Figure 17 illustrates battery charge and discharge profiles of a battery structure formed utilizing LiCoO₂ films according to embodiments of the present invention. The LiCoO₂ film in the battery profiled in Figure 17 was deposited according to Example 54 in Table I. The LiCoO₂ film was deposited on an alumina substrate with a gold current collector. The LiCoO₂ film was annealed utilizing a fast-ramp (45 sec) RTA process as was described above. A 1.5 µm LiPON layer was then deposited with a standard RF deposition process without bias in a modified AKT reactor. A lithium anode and a nickel current

collector were then deposited. Data was taken at 0.33 mA, 1.65 mA, 3.3 mA, 16.5 mA, 33 mA, and 66 mA. As observed, the battery was capable of storing an exceptional 25 mA/cm² at voltages greater than 2.0 V.

[0113] One skilled in the art will recognize variations and modifications of the examples specifically discussed in this disclosure. These variations and modifications are intended to be within the scope and spirit of this disclosure. As such, the scope is limited only by the following claims.

TABLE I

Example #	Target Power (kW)	Bias Power (W)	Reverse Time (μ s)	Frequency (kHz)	Ar (sccm)	O ₂ (sccm)	Initial Substrate Temperature (temperature during deposit) (°C)	Deposition Time (sec)	Film Thickness (μ m)
1	2	0	1.6	250	80	0	30	10000	3.9
2	2	0		250	72	8	30	7200	1.7
3	2	100		250	72	8	30	7200	1.34
4	2	100		250	76	4	30	7200	1.57
5	2	100		250	76	4	200	7200	1.3
6	2	100		250	74	6	200	7200	1.3
7	2	0		300	72	8	30	7200	1.58
8	2	0		300	74	6	30	7200	
9	2	100		300	74	6	30	7200	
10	2	100		300	72	8	30	7200	
11	2	100		300	70	10	30	7200	
12	2	0		300	70	10	30	7200	
13	2	0		300	72	8	30	7200	1.58
14	2	0		300	74	6	30	7200	
15	2	0		300	60	20	30	7200	
16	2	0		300	50	30	30	7200	
17	2	200		300	60	20	30	7200	
18	2	50		300	60	20	30	7200	
19	2	0		300	70	10	30	7200	
20	2	0		300	65	15	30	7200	
21	3	0		300	65	15	30	7200	
22	2	0	1.6	250	60	20	30	7200	
23	3	0	1.6	250	60	20	30	7200	
24	2	0	1.6	250	60	20	30 (NPH)	7200	

25	2	0	1.6	250	60	20	10min heat 30min coc	7200	
26	2	0	1.6	250	60	20	no preheat	9000	
27	2	0		300	60	20	no preheat	7200	
28	2	0		300	60	20	15min heat, 10min	7200	
29	2	0		250	60	20	no preheat		
30	2	0		250	60	20	10min, 10min		
31	2	0	1.3	300	60	20	30 (220)	7200	4.81
32	2	0	1.3	300	60	20	30 (220)	7200	4.74
33	2	0	1.3	300	22.5	7.5	30 (220)	7200	3.99
34	2	0	1.3	300	22.5	7.5	30 (220)	7200	3.93
35	2	0	1.3	300	37.5	12.5	30 (220)	7200	3.64
36	2	0	1.3	300	37.5	12.5	30 (220)	7200	3.54
37	2	100	1.3	300	60	20	30 (220)	7200	4.54
38	2	200	1.3	300	60	20	30 (220)	7200	4.84
39	2	100	1.3	300	37.5	12.5	30 (220)	7200	4.30
40	2	100	1.3	300	22.5	7.5	30 (220)	7200	3.77
41	2	200	1.3	300	37.5	12.5	30 (220)	7200	3.92
42	2	200	1.3	300	60	20	400	7200	3.77
43	2	0	1.3	300	22.5	7.5	30 (220)	7200	3.24
44	2	0	1.3	300	60	20	30 (220)	7200	3.88
45	2	0	1.3	300	60	20	30 (220)	3600	1.78
46	2	200	1.3	300	60	20	30 (220)	3600	1.87
47	2	200	1.3	300	22.5	7.5	30 (220)	3600	1.52
48	2	0	1.3	300	60	20	30 (220)	6000	1.12
49	2	0	1.3	300	60	20	30 (220)	10800	1.89
50	2	0	1.3	300	60	20	30 (220)	14400	2.52
51	2	100	1.3	300	60	20	30 (220)	10000	1.57
52	2	100	1.3	300	60	20	30 (220)	10000	2.11
53	2	100	1.3	300	60	20	30 (220)	6000	2.70

54	2	100	1.3	300	60	20	30(220)	6000	2.70
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TABLE II

Example #	Phase	Lattice	Texture	d ₁₀₁ [Å]	2θ [°]	crystallite size [Å]
15	LiCoO ₂	rhombohedral	strong [101]	2.376(1)	37.83	~1300
16	LiCoO ₂	Rhombohedral	strong [101]	2.375(1)	37.85	~750
17	Co	cubic	random	--	--	<50
18	Co	cubic	random	--	--	<50
19	LiCoO ₂	rhombohedral	strong [101]	2.370(1)	37.93	~1400
20	LiCoO ₂	rhombohedral	strong [101]	2.372(1)	37.90	~1500
21	LiCoO ₂	rhombohedral	strong [101]	2.370(1)	37.92	~1700
PDF	LiCoO ₂	Rhombohedral	random	2.408(1)	37.31	--

WHAT IS CLAIMED IS:

1. A method of depositing a LiCoO_2 layer, comprising:
placing a substrate in a reactor;
flowing a gaseous mixture including argon and oxygen through the reactor; and
applying pulsed DC power to a target formed of LiCoO_2 positioned opposite the
substrate,
wherein a crystalline layer of LiCoO_2 is deposited over the substrate.
2. The method of claim 1, further including applying an RF bias to the substrate.
3. The method of claim 1, wherein the crystalline layer is $\langle 101 \rangle$ oriented.
4. The method of claim 1, wherein the crystalline layer is $\langle 003 \rangle$ oriented.
5. The method of claim 1, wherein a grain size of the crystalline layer is between
about 750 Å and about 1700 Å.
6. The method of claim 1 wherein the substrate is a material chosen from a set
comprised of silicon, polymers, glasses, ceramics, and metals.
7. The method of claim 1, further including preheating the substrate to a temperature
of about 200 °C.
8. The method of claim 1, wherein the substrate is a low temperature substrate.
9. The method of claim 8, wherein the low temperature substrate is one of a set of
substrates including glass, plastic, and metal foil.
10. The method of claim 1, further including depositing an oxide layer on the
substrate.
11. The method of claim 10, wherein the oxide layer is a silicon dioxide layer.
12. The method of claim 3, wherein the crystalline layer is deposited at a rate of
greater than 1 μm per hour.

13. The method of claim 1 wherein the target is a ceramic LiCoO_2 sputter target with a resistance measured across about 4 cm of surface of less than about 500 k Ω .
14. The method of claim 1, further including depositing a metal layer on the substrate.
15. The method of claim 14, wherein the metal layer is iridium.
16. The method of claim 14, wherein the metal layer is platinum.
17. The method of claim 1, further including annealing the crystalline layer with a low thermal budget.
18. The method of claim 17, wherein annealing the crystalline layer includes annealing to 700°C in a rapid thermal anneal process for a period of time less than about 10 minutes.
19. The method of claim 14, further including annealing the LiCoO_2 layer at a temperature of less than or equal to about 500°C.
20. The method of claim 14, further including annealing the LiCoO_2 layer at a temperature of less than or equal to about 400°C.
21. A battery structure, comprising:
 - a crystalline LiCoO_2 layer deposited over a low-temperature substrate.
22. The structure of claim 21, further including a conducting layer deposited between the crystalline LiCoO_2 layer and the low-temperature substrate.
23. The structure of claim 22, wherein the conducting layer is an iridium layer.
24. The structure of claim 22, wherein the conducting layer is a platinum layer.
25. The structure of claim 21, further including a LiPON layer deposited over the LiCoO_2 layer.
26. The structure of claim 21, further including a second conducting layer deposited over the LiCoO_2 layer.

27. A stacked battery structure, comprising:

one or more battery stacks deposited on a thin substrate, wherein each battery stack comprises:

a conducting layer,

a LiCoO_2 layer deposited as a crystalline layer over the conducting layer,

a LiPON layer deposited over the crystalline LiCoO_2 layer,

an anode layer deposited over the LiPON layer; and

a top conducting layer deposited over the one or more battery stacks.

28. The stacked battery structure of claim 27, wherein the battery stacks form a parallel stacked battery structure.

29. The stacked battery structure of claim 27, wherein the battery stacks form a series stacked battery structure.

30. The stacked battery structure of claim 27, wherein the conducting layer is a metal layer deposited on a substrate.

31. The stacked battery structure of claim 30, wherein the metal layer is an iridium layer.

32. The stacked battery structure of claim 30, wherein the metal layer is a platinum layer.

33. The stacked battery structure of claim 30, wherein the substrate is a low temperature substrate.

34. The stacked battery structure of claim 27, wherein the conducting layer is a metallic foil.

35. The stacked battery structure of claim 34, wherein the metallic foil is formed of a metal from a group consisting of copper, gold, platinum, aluminum, stainless steel and other nickel or cobalt based super alloy.

36. A method of producing a battery, comprising:

loading a substrate into a cluster tool;

depositing a crystalline LiCoO_2 layer over a conducting layer in a chamber of the cluster tool with a pulsed-dc PVD process.

37. The method of claim 36, wherein depositing a crystalline LiCoO_2 layer includes depositing crystalline LiCoO_2 through a mask.

38. The method of claim 36, further including

depositing a conducting layer on the substrate.

39. The method of claim 36, further including depositing a LiPON layer over the LiCoO_2 layer.

40. The method of claim 39, further including deposition an anode over the LiPON layer.

41. The method of claim 40, further including depositing a conducting layer over the anode.

42. The method of claim 36, wherein the conducting layer is an iridium layer.

43. A fixture for holding a thin substrate, comprising:

a top portion; and

a bottom portion, wherein

the thin substrate is held when the top portion is attached to the bottom portion.

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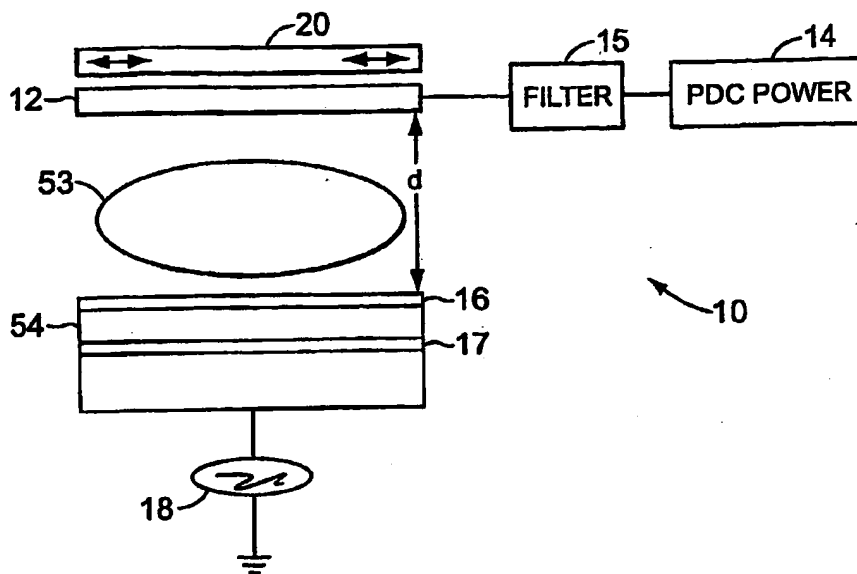


FIG. 1A

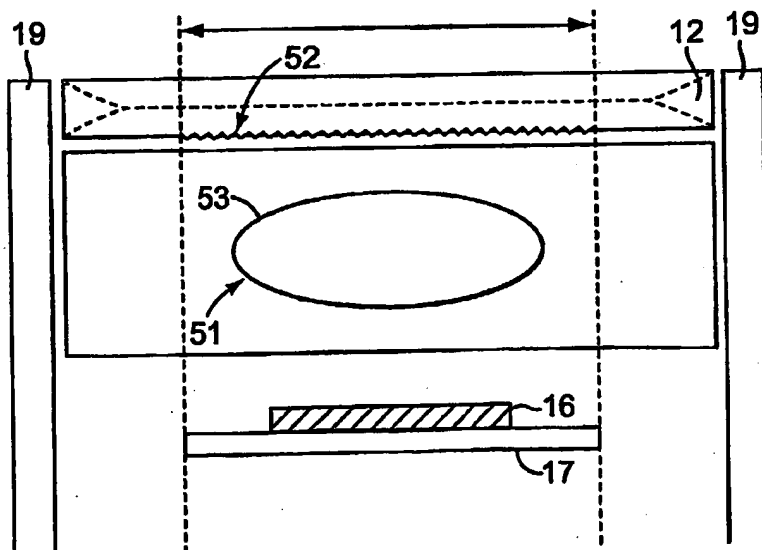


FIG. 1B

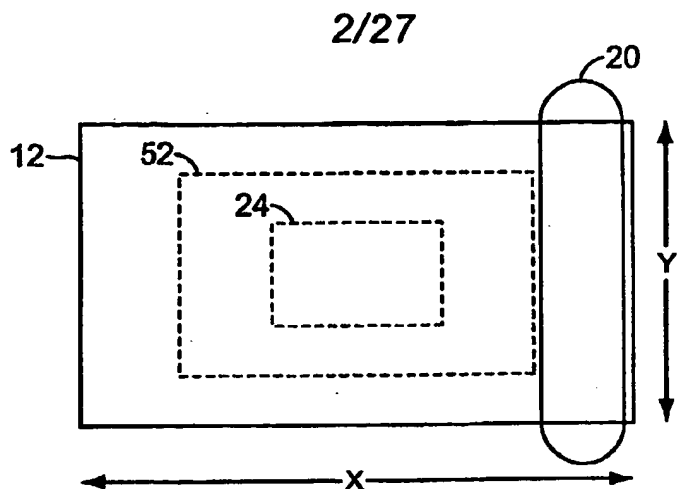


FIG. 2

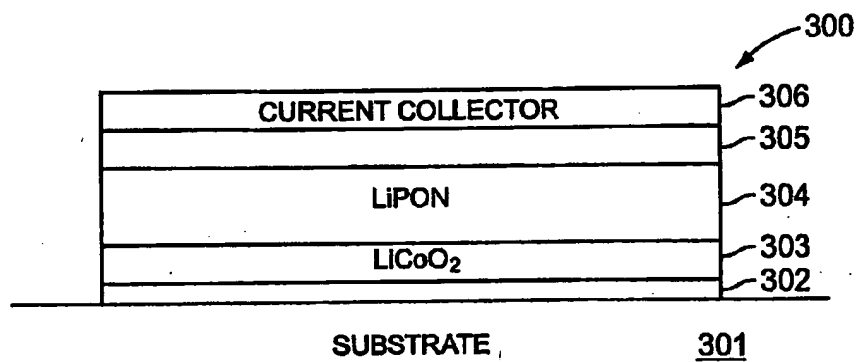


FIG. 3

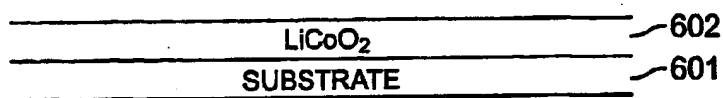


FIG. 6A

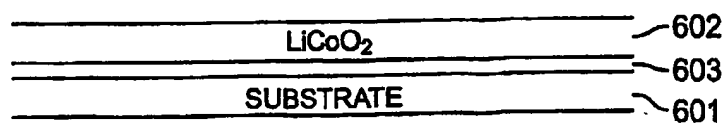


FIG. 6B

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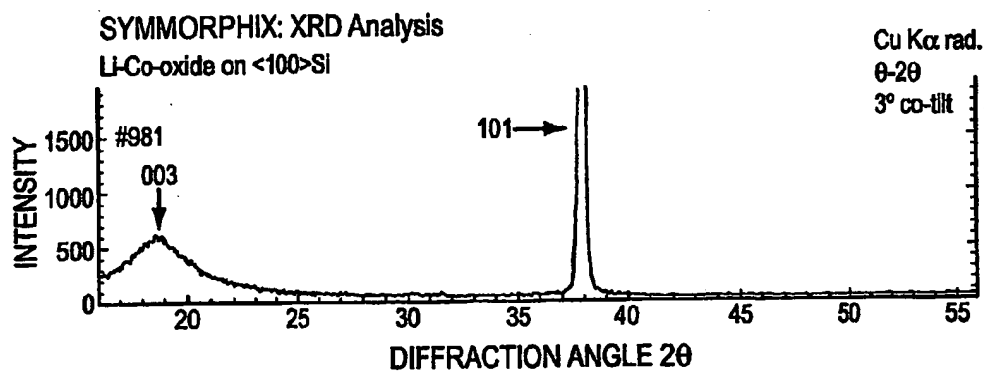


FIG. 4A

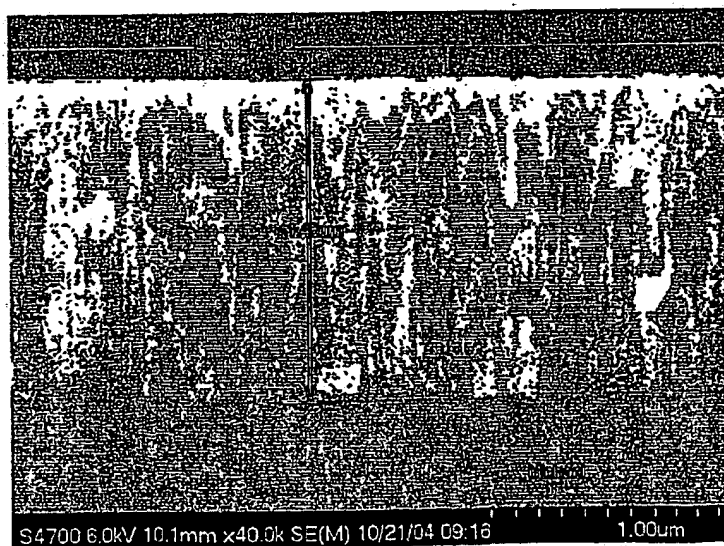


FIG. 4B

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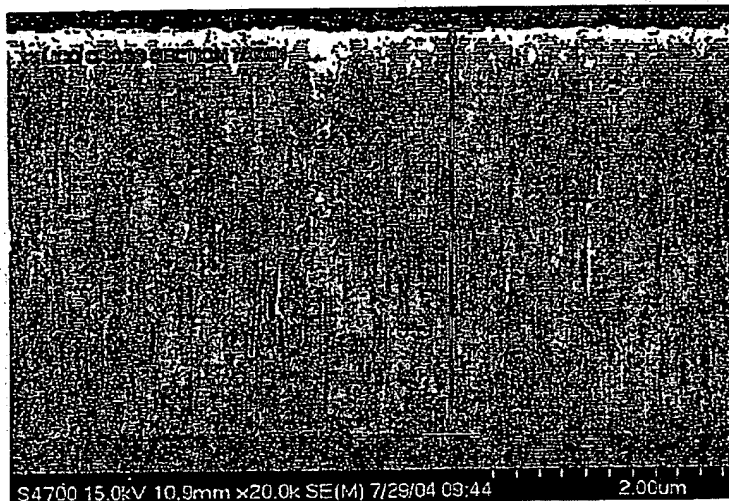


FIG. 5A

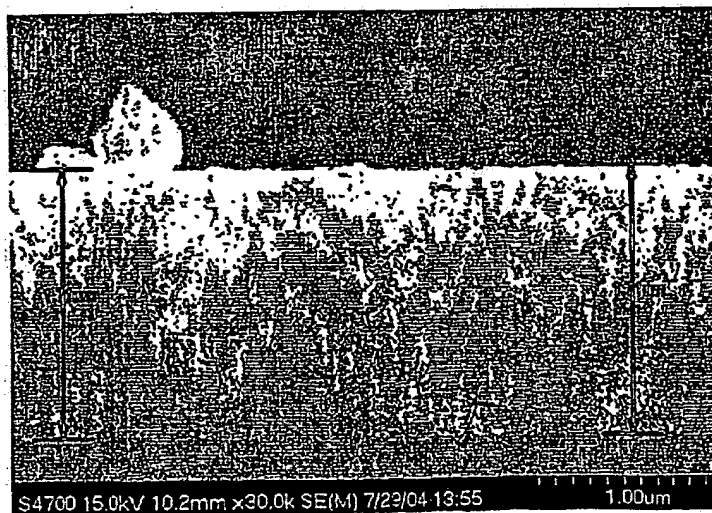
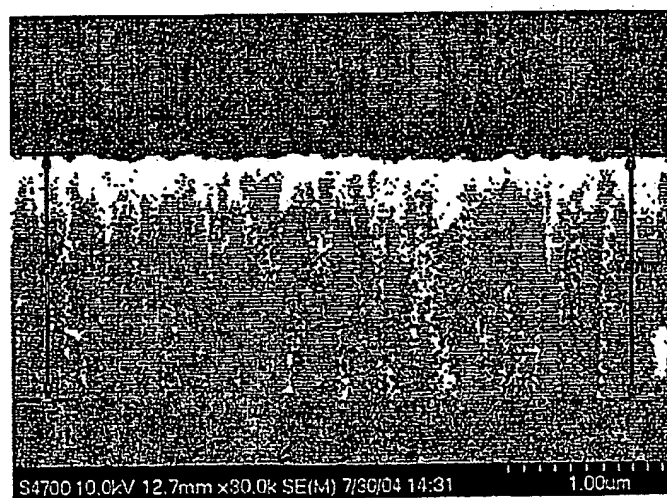
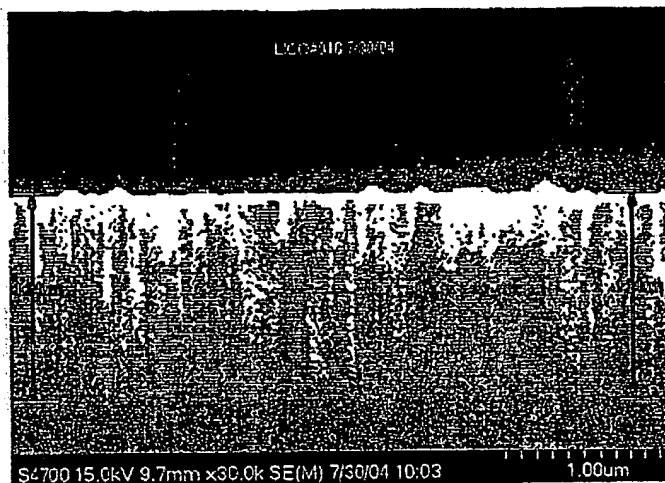


FIG. 5B

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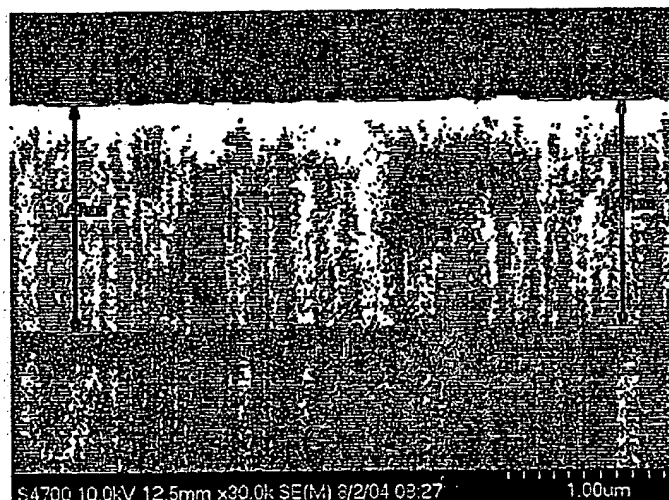


FIG. 5E

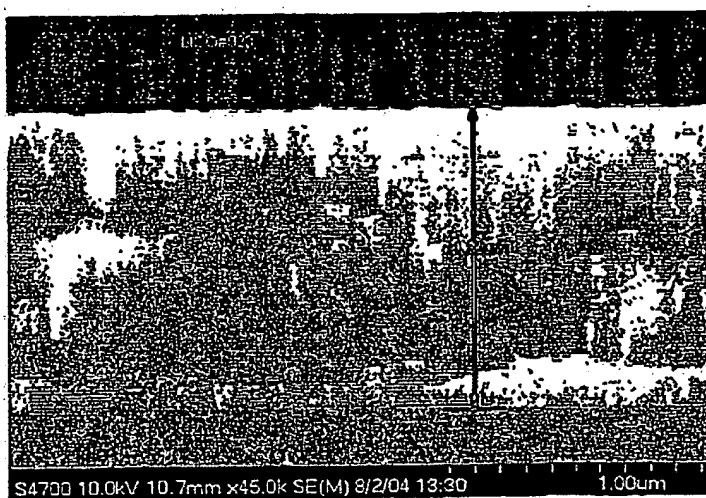
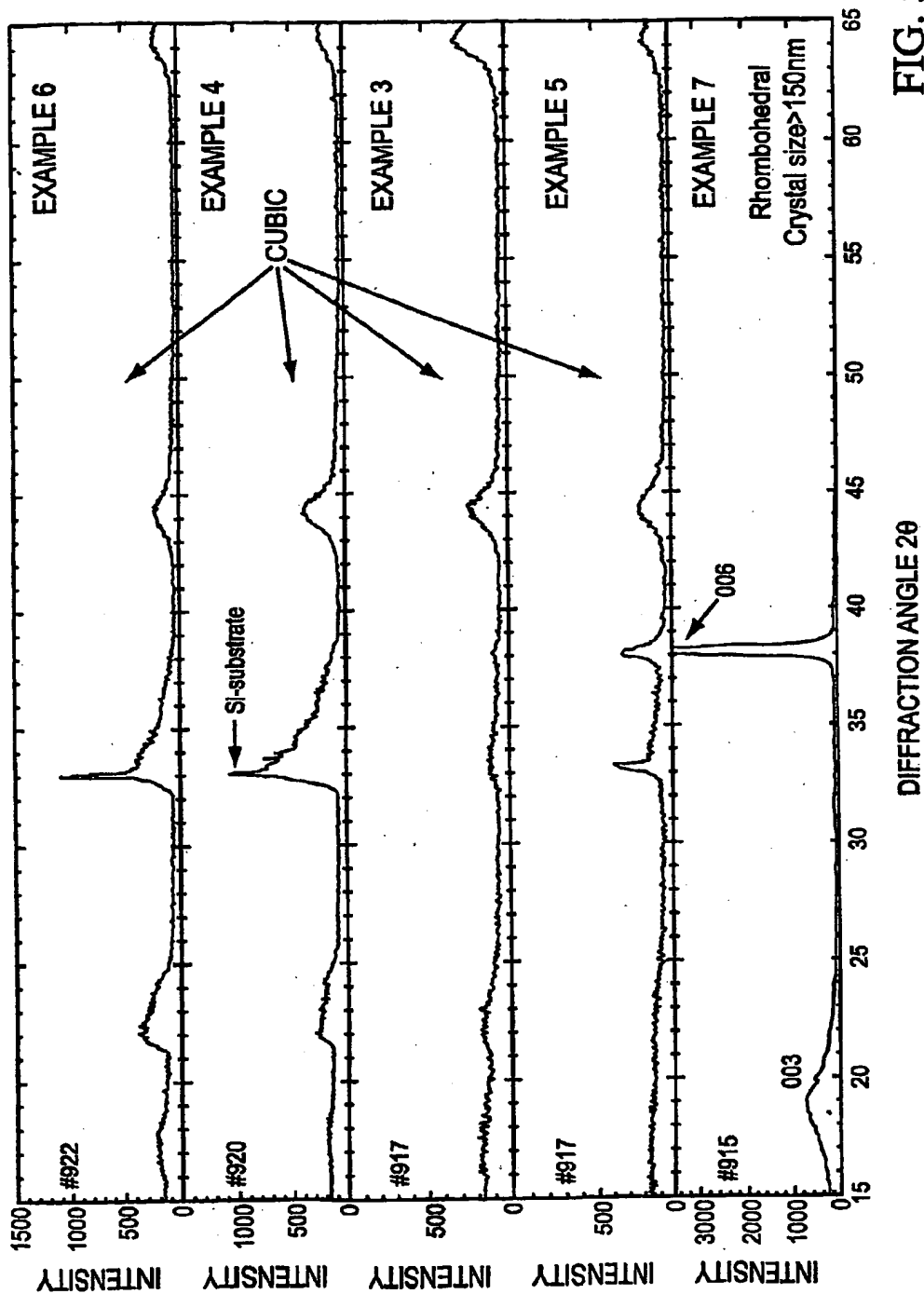


FIG. 5F

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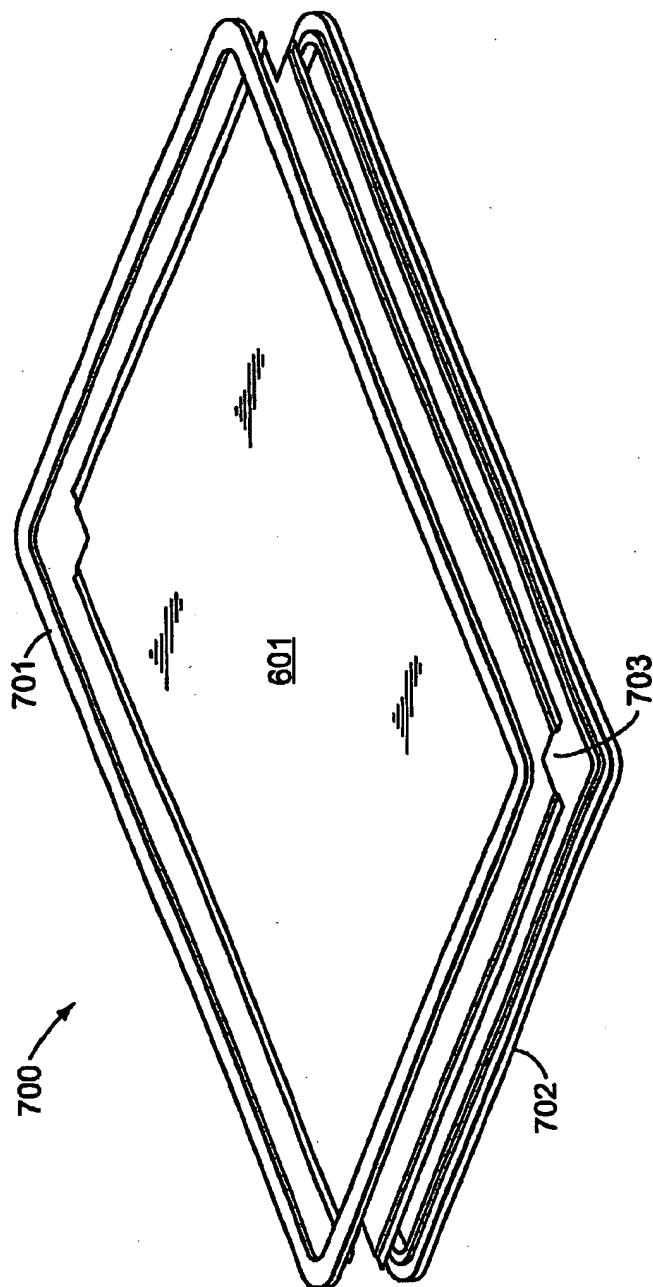
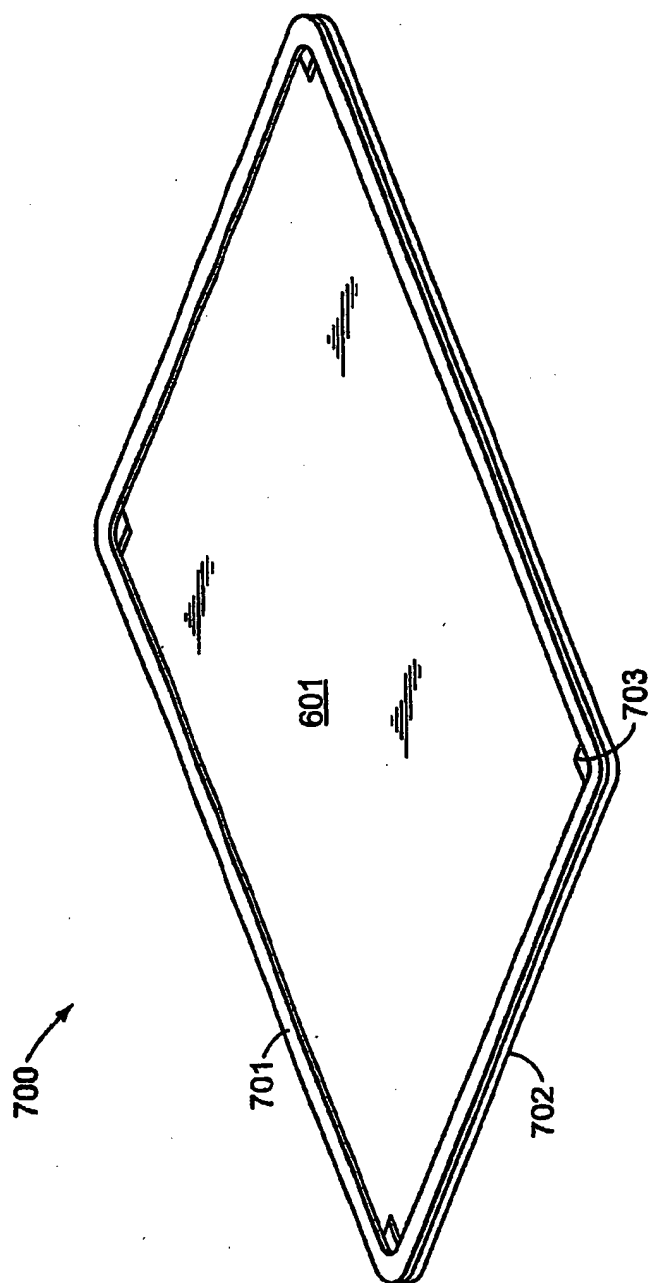


FIG. 7A

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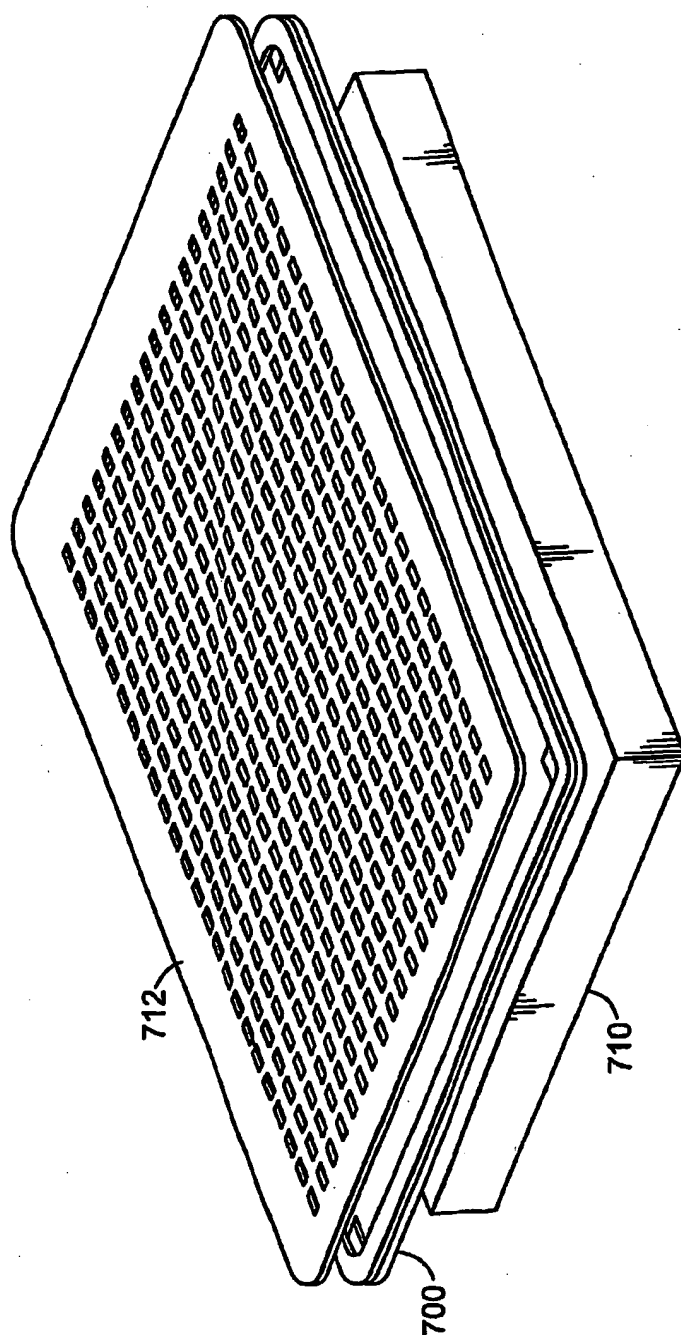


FIG. 7C

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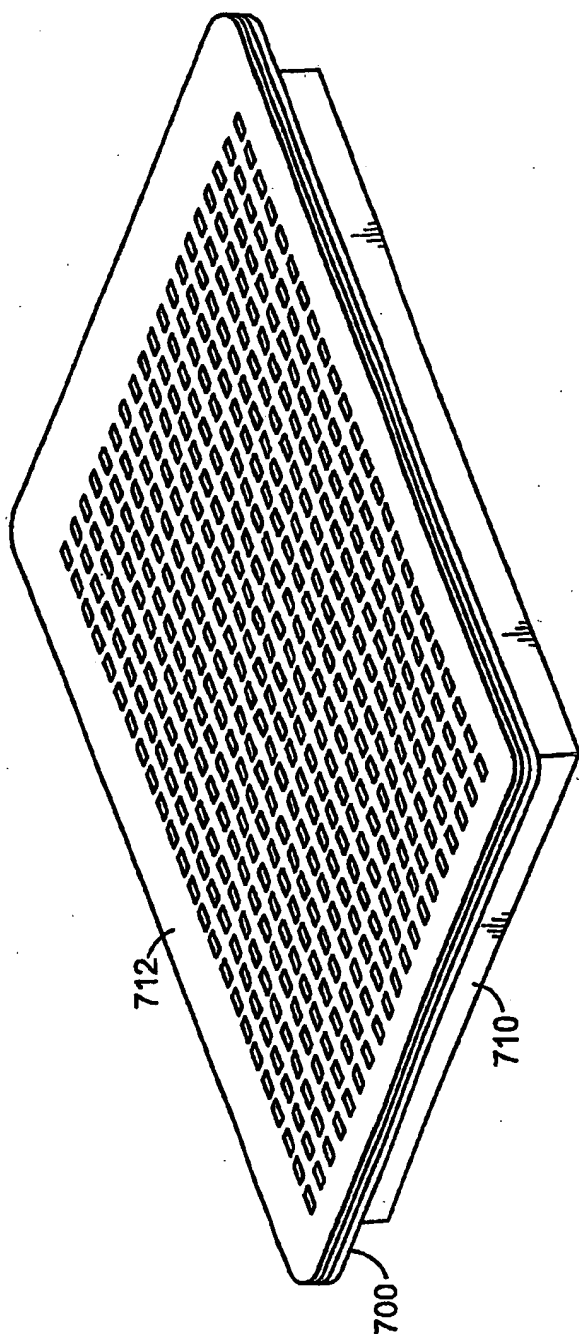


FIG. 7D

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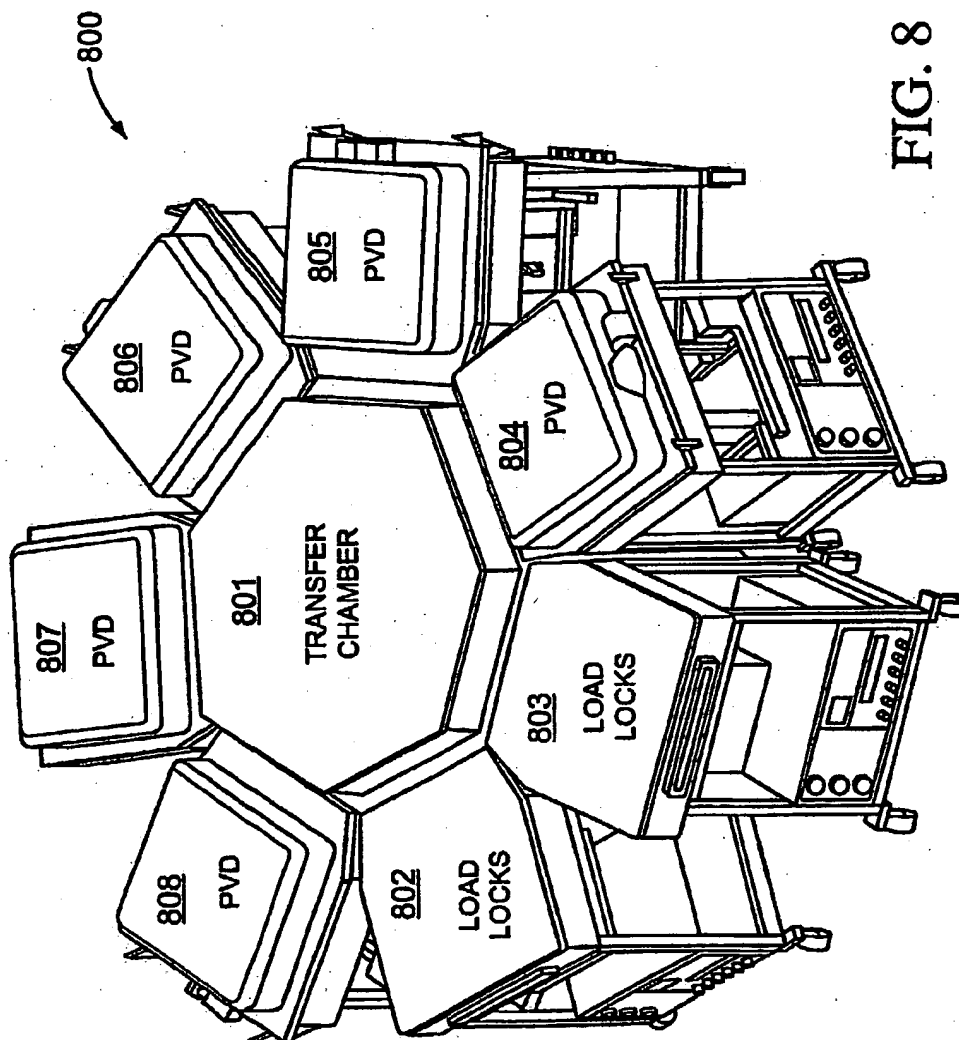


FIG. 8

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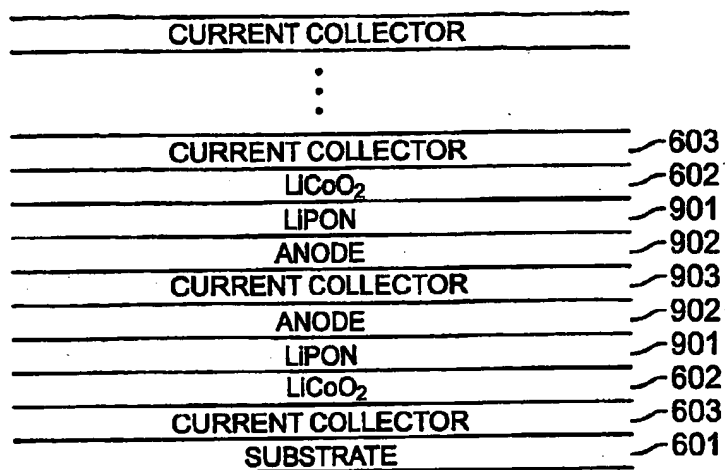


FIG. 9A

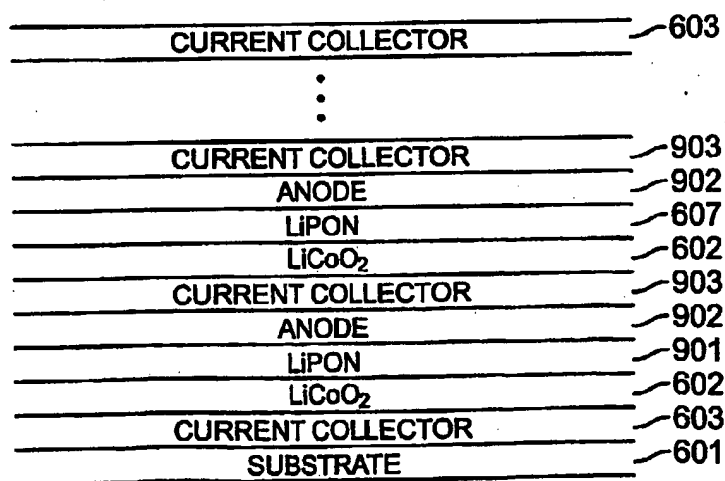
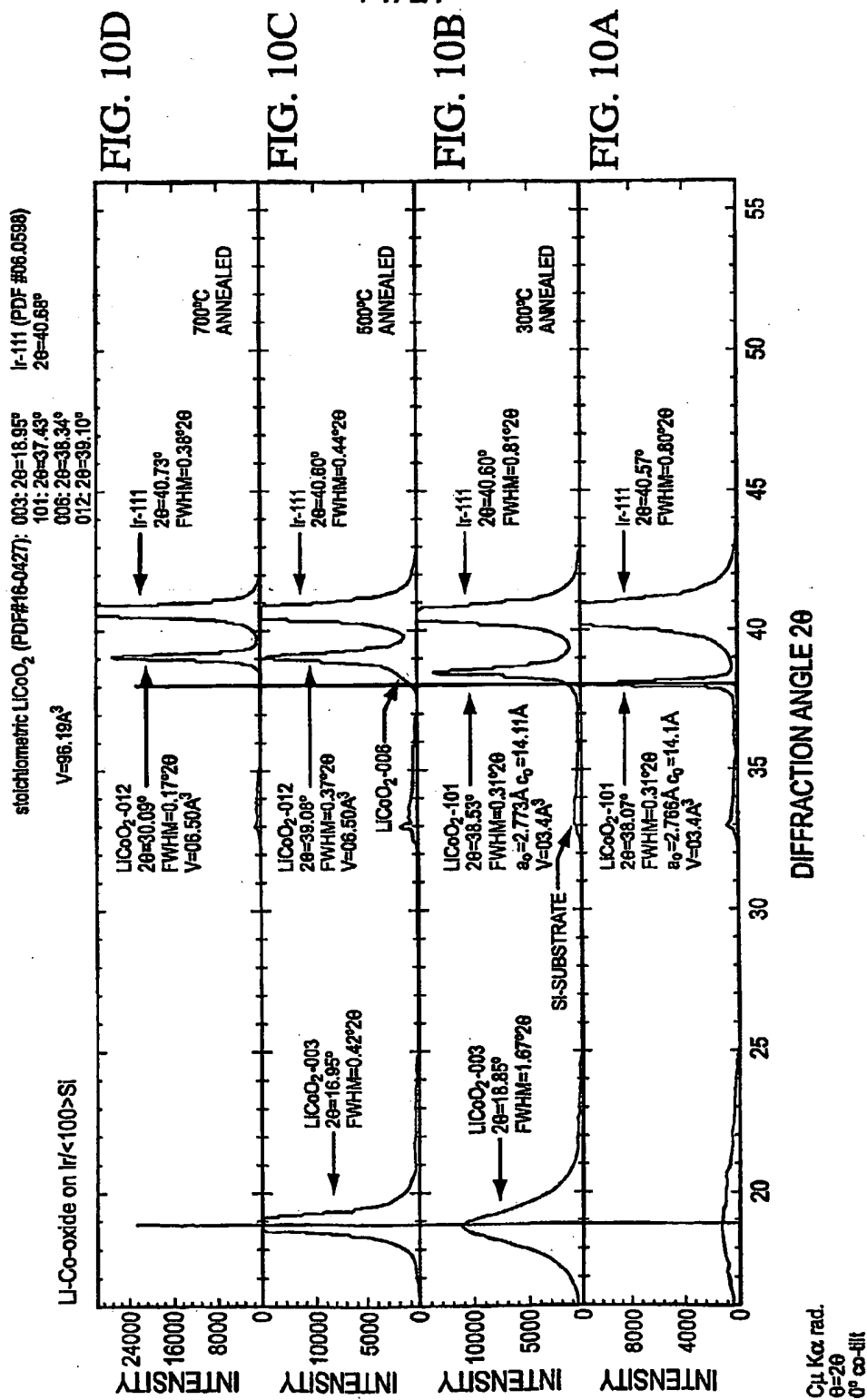


FIG. 9B

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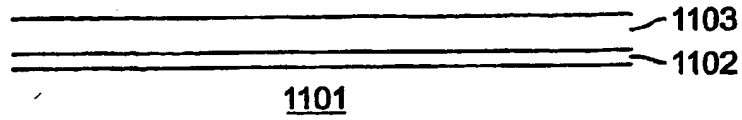


FIG. 11A

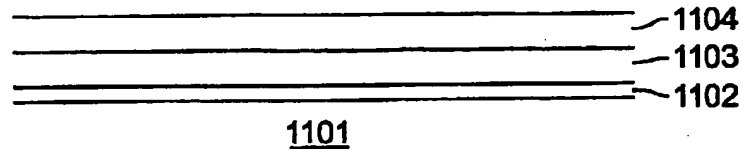


FIG. 11B

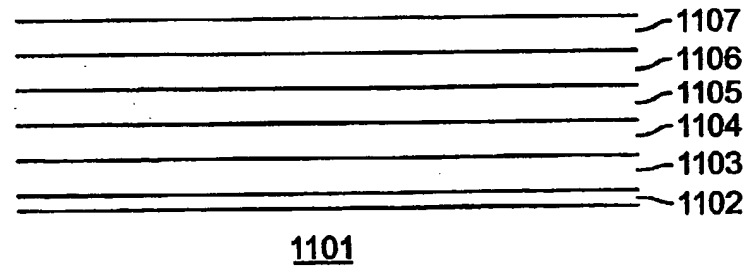


FIG. 11C

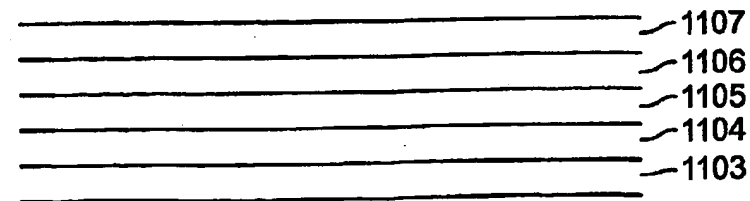


FIG. 11D

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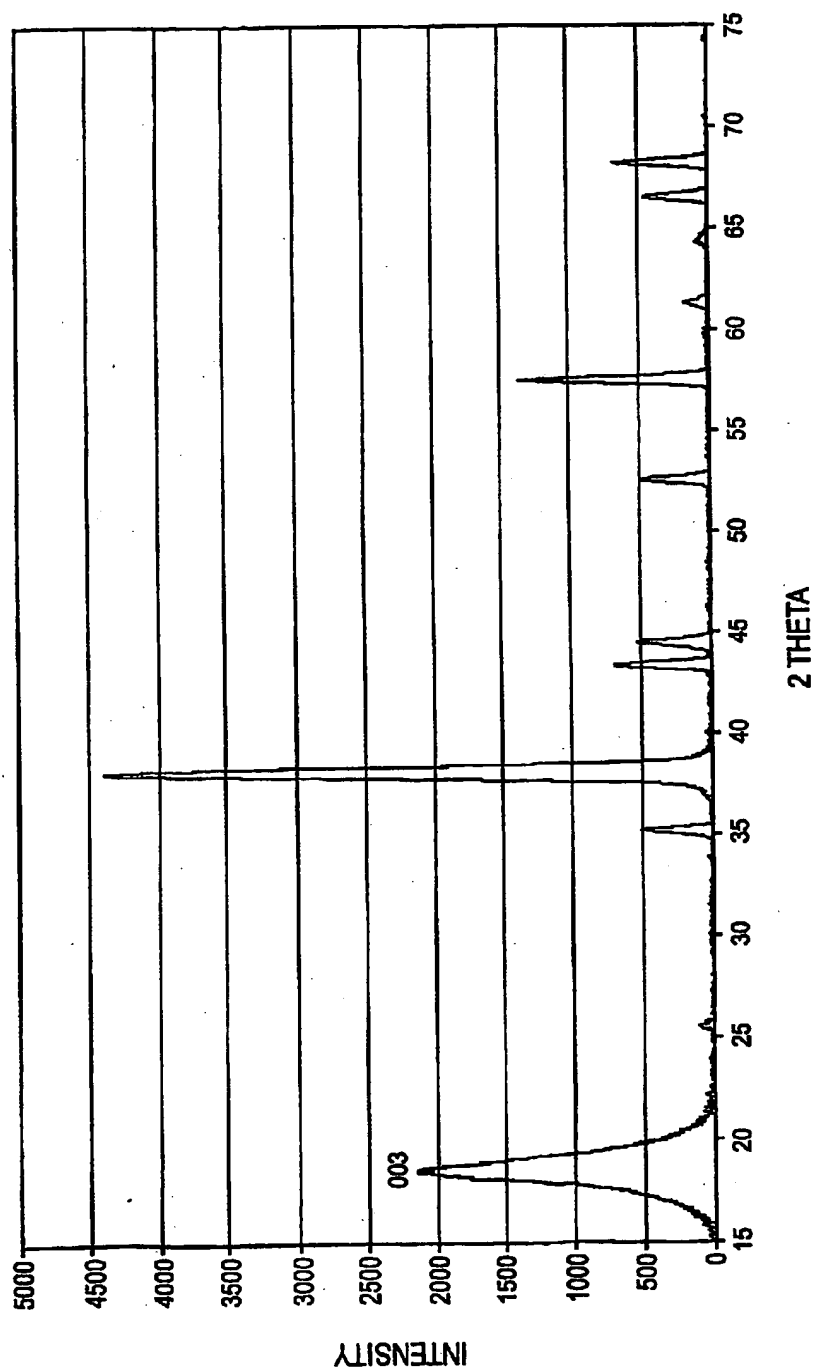


FIG. 12A

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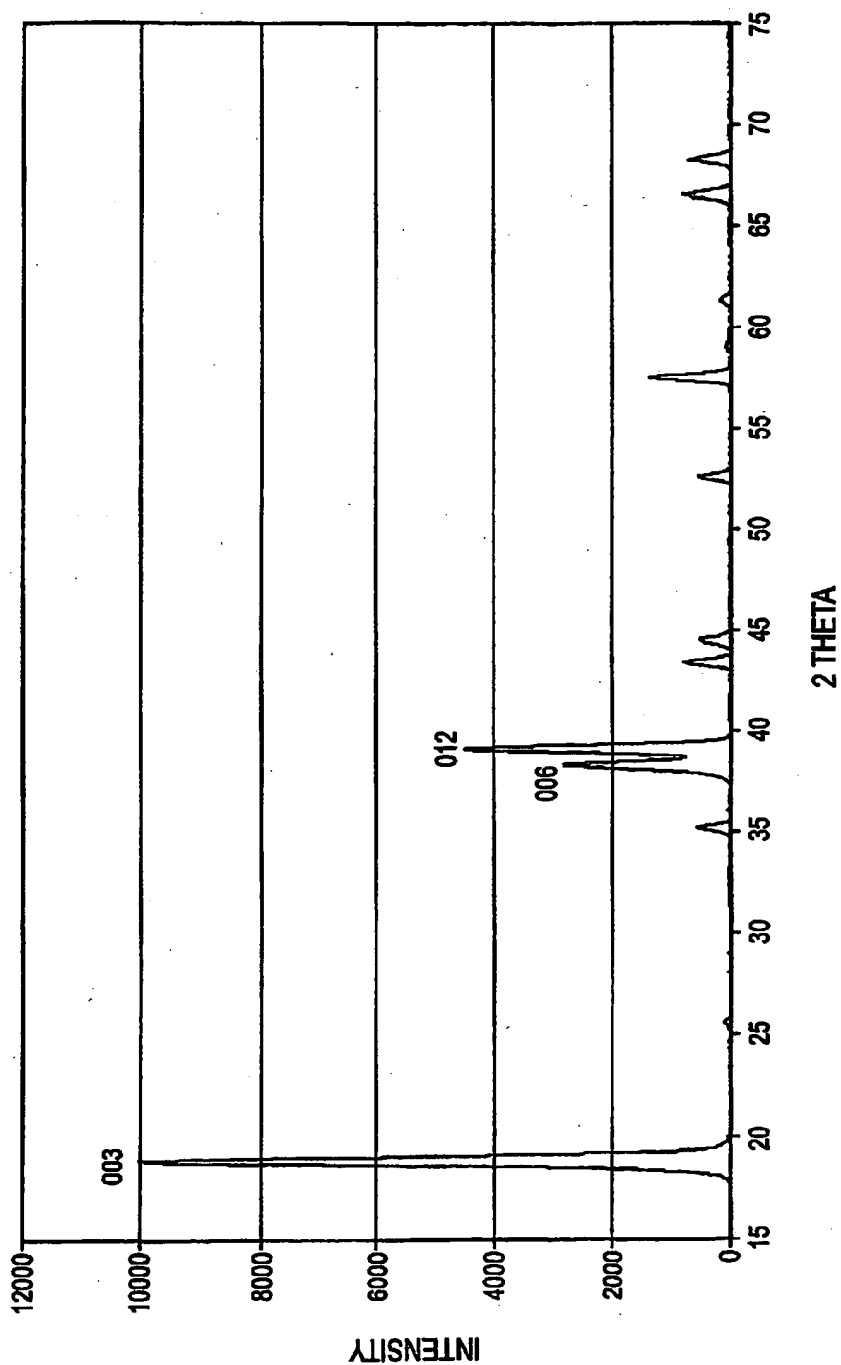


FIG. 12B

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FIG. 12D

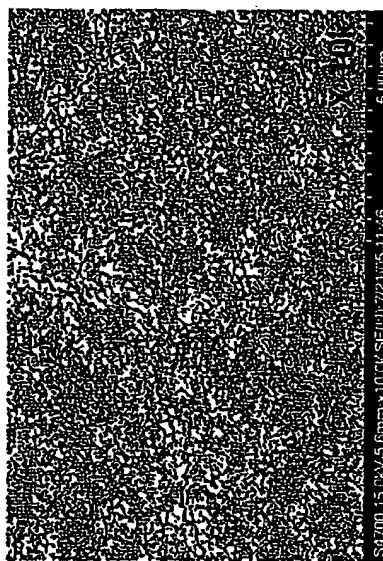


FIG. 12F



FIG. 12C



FIG. 12E

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FIG. 12H

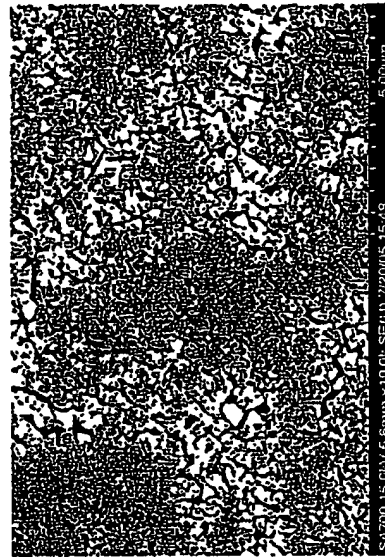


FIG. 12J

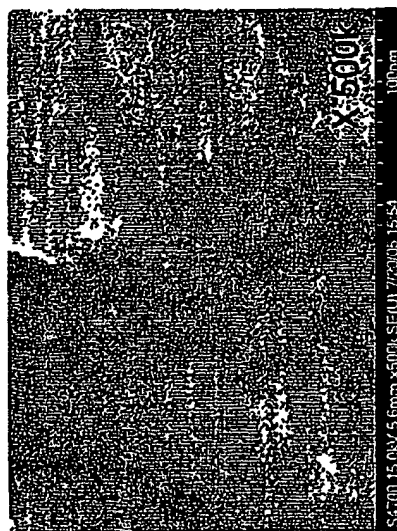


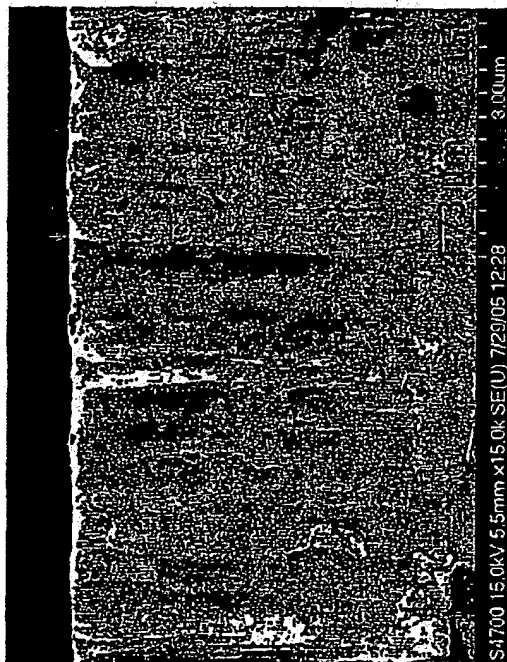
FIG. 12G



FIG. 12I

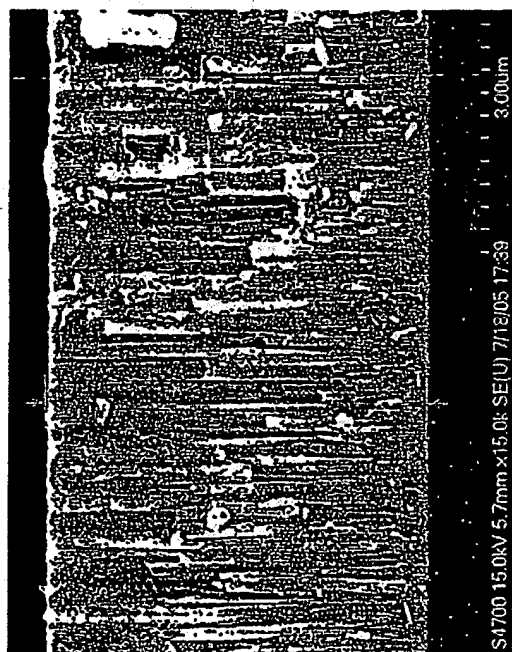
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FIG. 12L



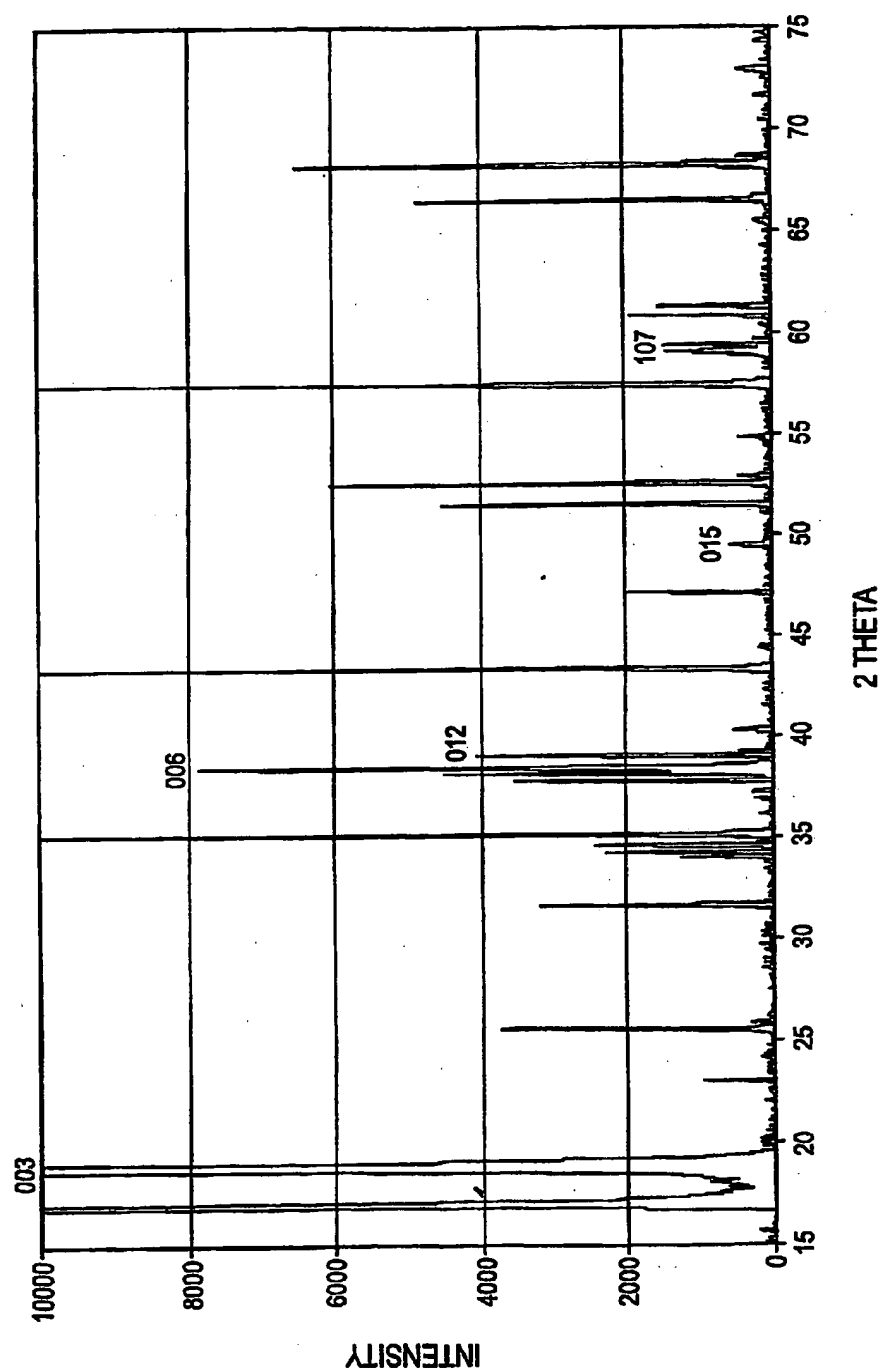
On alumina

FIG. 12K



On Si

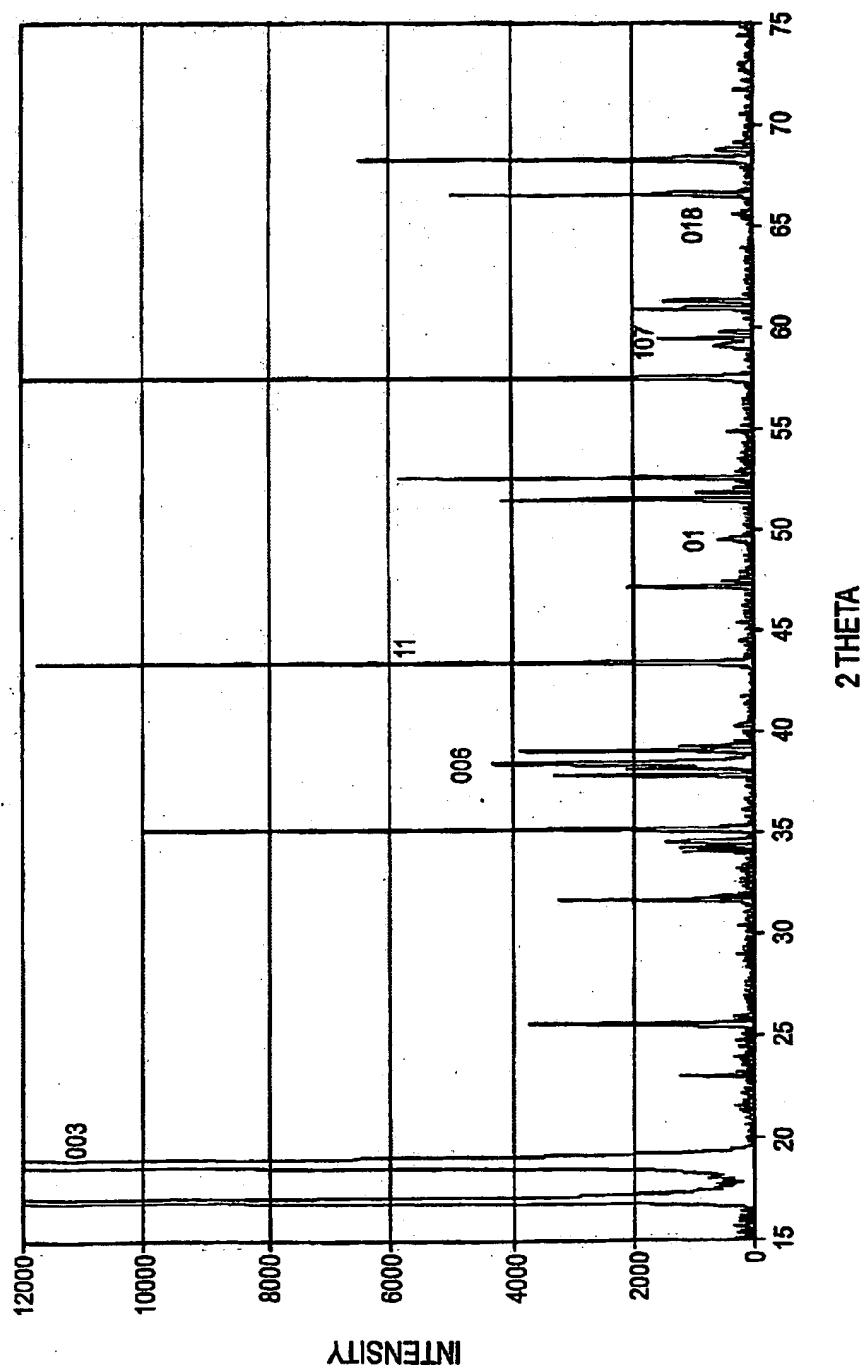
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2 THETA

FIG. 13A

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2 THETA

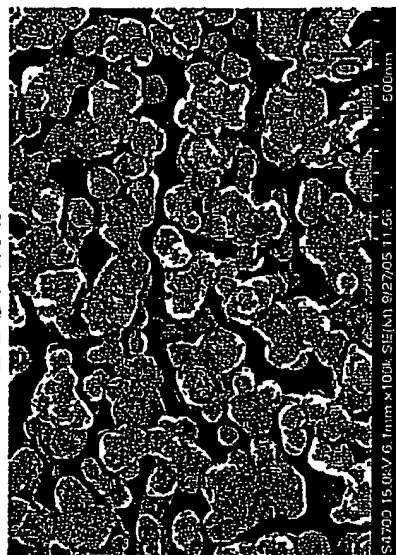
FIG. 13B

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FIG. 13E



FIG. 13F



In Ar/O₂ (3/1)

FIG. 13C



FIG. 13D



In Ar

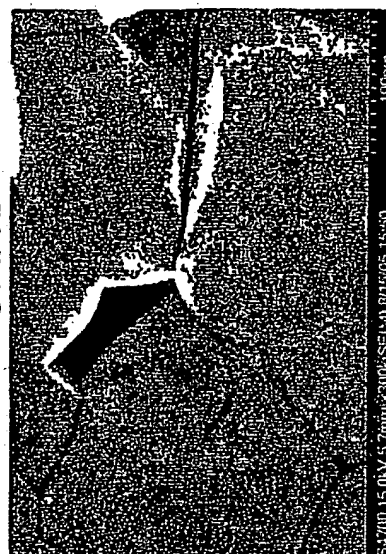
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FIG. 14B



700CX2h

FIG. 14D



RTA-700C15m

FIG. 14A



As deposited

FIG. 14C



RTA-5m

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FIG. 15A

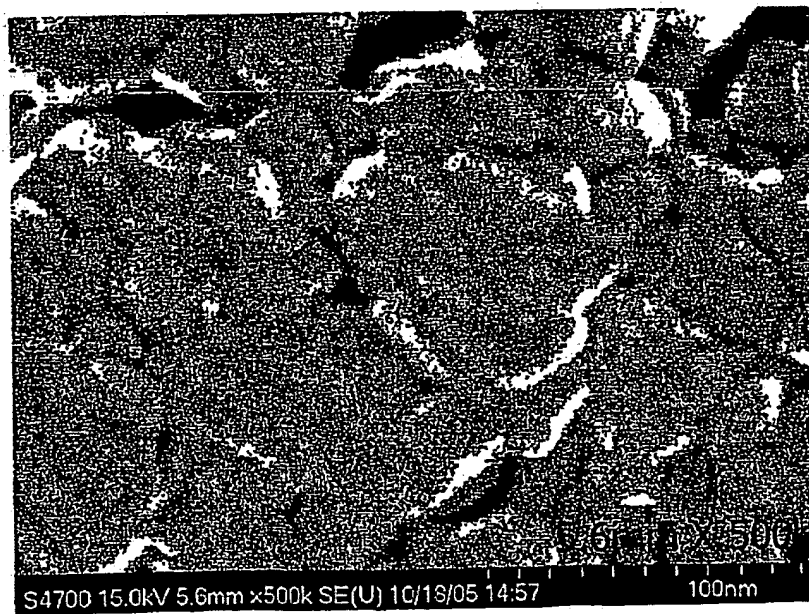
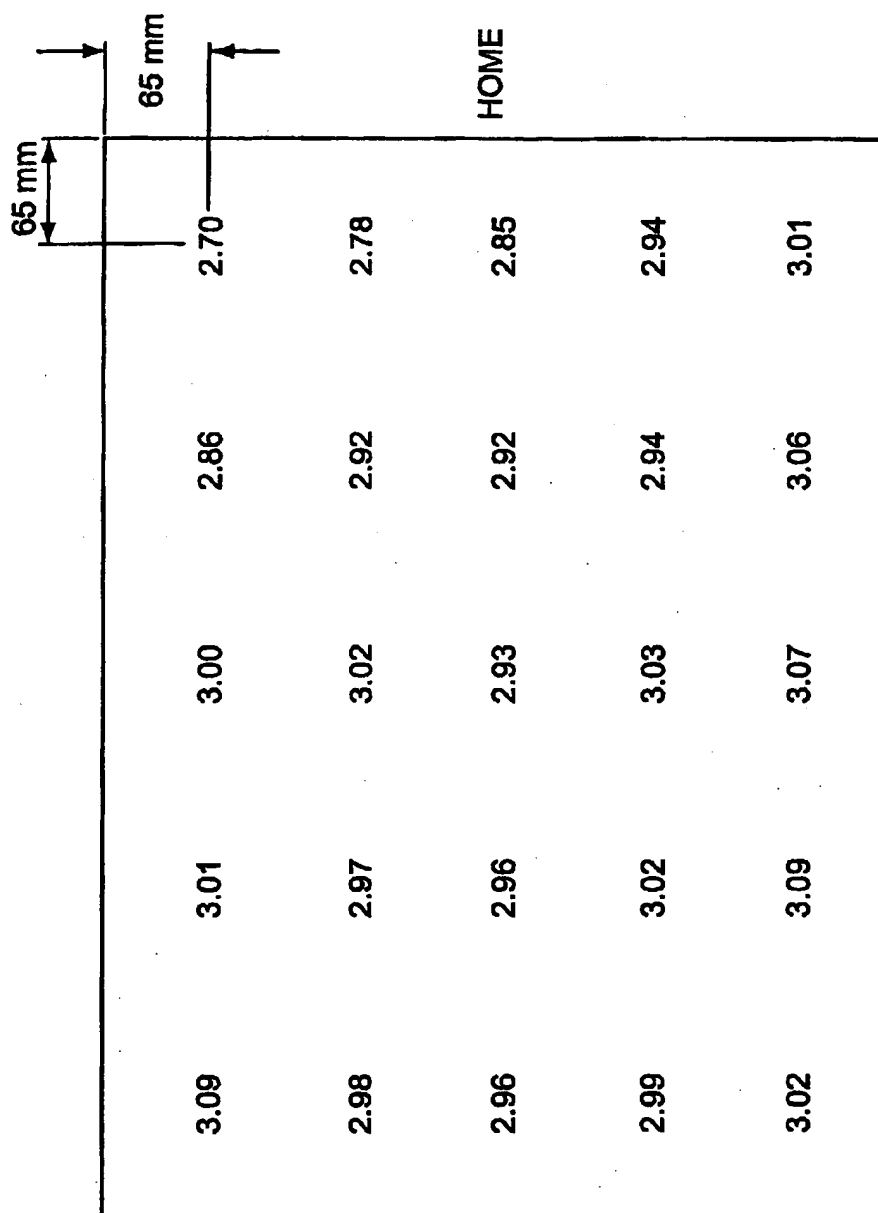


FIG. 15B

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The diagram shows a rectangular array of numerical data. Above the array, there are two horizontal dimension lines, each labeled "65 mm". The first dimension line spans the width of the first two columns of the array. The second dimension line spans the width of the last two columns. To the right of the array, the word "HOME" is written vertically. The array itself consists of five rows and six columns of numbers.

3.09	3.01	3.00	2.86	2.70	
2.98	2.97	3.02	2.92	2.78	
2.96	2.96	2.93	2.92	2.85	
2.99	3.02	3.03	2.94	2.94	
3.02	3.09	3.07	3.06	3.01	

FIG. 16

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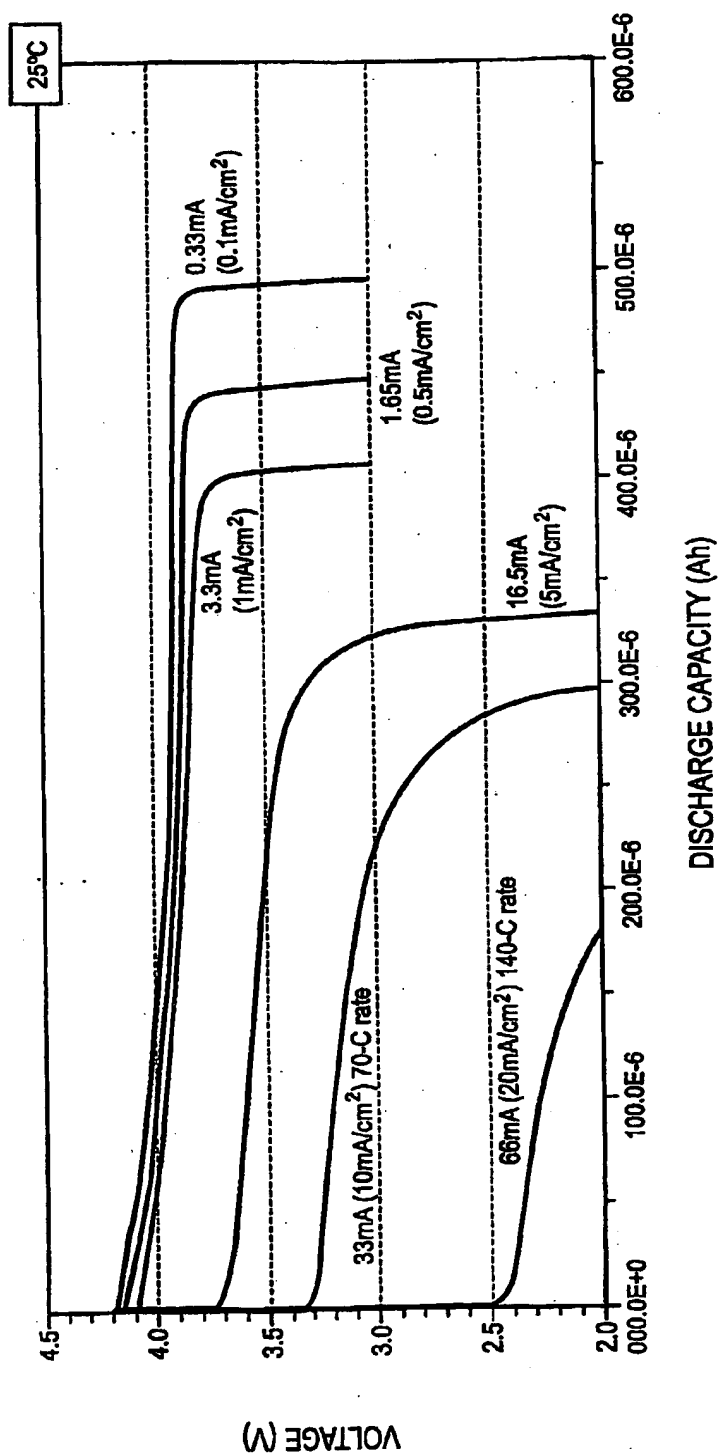


FIG. 17

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